# MAM2026

MARCH 23-26 • CHEMNITZ (GERMANY)

# ABSTRACTS BOOK

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# FOREWORD

On behalf of the Organising and Scientific Committees, we take great pleasure in welcoming you to this new edition of the Materials for Advanced Metallization International Conference (MAM2026).

MAM 2026 marks the 33rd edition of this prestigious conference series dedicated to materials, processes, and their integration within front-end and back-end microelectronics. Established in the 1980s as a workshop on refractory metals and silicides, the conference has evolved significantly since 1995. Its scope now encompasses advanced materials for metallization, memory and memristive devices, 1D/2D nanomaterials, as well as 2D and 3D packaging solutions. Furthermore, the program emphasizes specialized characterization and modeling techniques, including advanced analytics, reliability and failure analysis, and process simulation. The applications are multifaceted, covering CMOS-based microelectronics, power semiconductors, alternative memory technologies, spintronic, neuromorphic, and quantum devices, sensors, actuators, 3D integration, and SOC/SIP architectures.

The conference aims to provide an international forum for in-depth discussion on fundamental and applied sciences alongside industrial applications. It is designed for scientists, process and integration engineers, R&D managers, and doctoral candidates.

### Chemnitz: A Hub of Innovation, Tradition, and Culture

MAM 2026 takes place in Chemnitz, European Capital of Culture 2025 — a city where deep-rooted industrial heritage meets cutting-edge future technologies. Founded in 1143, Chemnitz established an early tradition in textile crafting during the late Middle Ages, notably through the 'Bleichprivileg' (bleaching privilege) of 1357. However, it was during the 19th century that the city rose to international prominence as a powerhouse of the Industrial Revolution, eventually earning the nickname 'the Manchester of Saxony.'

The city is the birthplace of numerous world-changing innovations: it was here that Richard Hartmann revolutionized locomotive construction and the Thermos flask (vacuum flask) was invented by Reinhold Burger. Furthermore, Chemnitz saw the development of the mechanical weaving loom and the world’s first mild detergent (Fewa).

Today, Chemnitz is a cornerstone of 'Silicon Saxony,' Europe’s largest microelectronics cluster. The city’s scientific profile is shaped by the Chemnitz University of Technology (TU Chemnitz) and renowned research institutes like Fraunhofer ENAS, specializing in Smart Systems Integration, Micro and Nanosystems, and advanced materials science. Economically, the region serves as a driver of innovation in microelectronics, microsystems technology, and hydrogen research, offering a vibrant ecosystem of global players and specialized SMEs.

This visionary spirit is mirrored in the city’s urban landscape. Chemnitz boasts the Kaßberg district, one of Europe’s largest contiguous residential areas featuring a magnificent blend of Wilhelminian-style (Gründerzeit) and Art Nouveau (Jugendstil) architecture. Visitors can admire opulent facades and gems like the Villa Esche, designed by the Belgian master Henry van de Velde. Alongside modern landmarks like the iconic Karl Marx Monument and the medieval Red Tower, Chemnitz provides an inspiring and unique backdrop for the international guests of MAM 2026.

The conference will be opened with keynote by Claire Fenouillet-Beranger from CEA-LETI, focusing on key building blocks driving the development of the 10nm FD-SOI node. Her presentation highlights critical technological advancements in the field. The invited talks feature international experts addressing topics of on advanced packaging, heterogeneous integration, metallization, and simulation as well as laser processing, advanced characterization and integration. They will be given by speakers from industry and research organizations including 3D-Micromac, MKS-Atotech, Institute of Science Tokyo, Applied Materials, Confovis, CEA-LETI, STMicroelectronics, imec, and TU Chemnitz/Fraunhofer ENAS. Complementing these highlights, the program features a wide array of oral and poster presentations that offer a deep dive into fundamental and applied research, ensuring a vibrant and multi-faceted exchange of ideas.

Prior to the technical sessions of MAM2026, a workshop will spotlight "Technologies for Heterointegration and Chiplets", two of the most critical drivers for the future of high-performance computing and modular system design. Technologies for heterogeneous integration and chiplets focus on breaking down large, monolithic chips into smaller, specialized, functional dies (chiplets) and reassembling them using advanced packaging to achieve higher performance, lower power consumption, and improved yield. Additionally, this approach enables functional diversification by integrating logic, memory, analog, sensors, and even photonics in a single package. Key technologies driving this shift include 2.5D/3D integration, hybrid bonding, and novel interposer materials. The workshop features deep-dive sessions led by international experts from world-leading research hubs.

We are indebted to Confovis, JX Advanced Metals, Infineon, Von Ardenne and ErzM-Technologies for their financial support. Furthermore, we are grateful to the Phantoms Foundation for their organisation and logistical support. Lastly, we also would like to thank all the speakers, poster presenters, exhibitors (Confovis, JX Advanced Metals, Infineon. Von Ardenne, Kurt J. Lesker Company, scia Systems and Polyteknik AS) and participants that joined us in person this year to make the conference a success.

Hope to see you again in the next edition of MAM.

**Stefan E. Schulz** - General Chair MAM2026

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The company was founded in 2015 by Knut Gottfried, head surface processing at the Fraunhofer Institute ENAS in Chemnitz. He is also chairman of the European CMP & WET Users Group.
Due to worldwide connections to semiconductor suppliers, institutes and companies ErzM-Technologies provides a great network of solutions. ErzM-Technologies offers strategy guidance, process and technology development and foundry services along the full semiconductor chip cycle, such as CMP, Wet Processing, ECD, Plasma Processing, Lithography, Wafer Level Packaging / Bonding and a broad variety of Wafer Characterization techniques.

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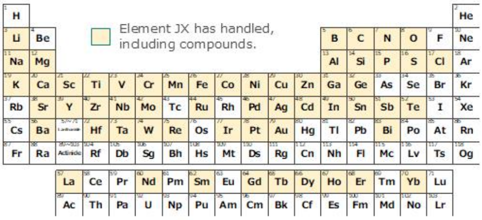
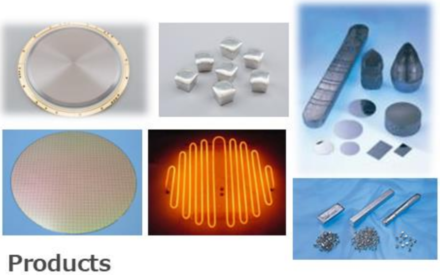
### Thin Film Deposition Materials

- Barriers & liners
- Interconnect
- Silicide and gate
- Phase-change & magnetic memory
- Magnetic sensors
- MEMS & RF
- RDL, TSV, TGV
- Top and bottom electrodes
- Si photonics, EUV masks & optical
- Piezo-electronics
- Super-computing





### Products

- Sputtering targets, coils, plating anodes
- Cd, Te, and In 6N-7N high purity metals for epitaxy as shots, flakes, crucibles
- InP and CdZnTe wafers and YAG crystals
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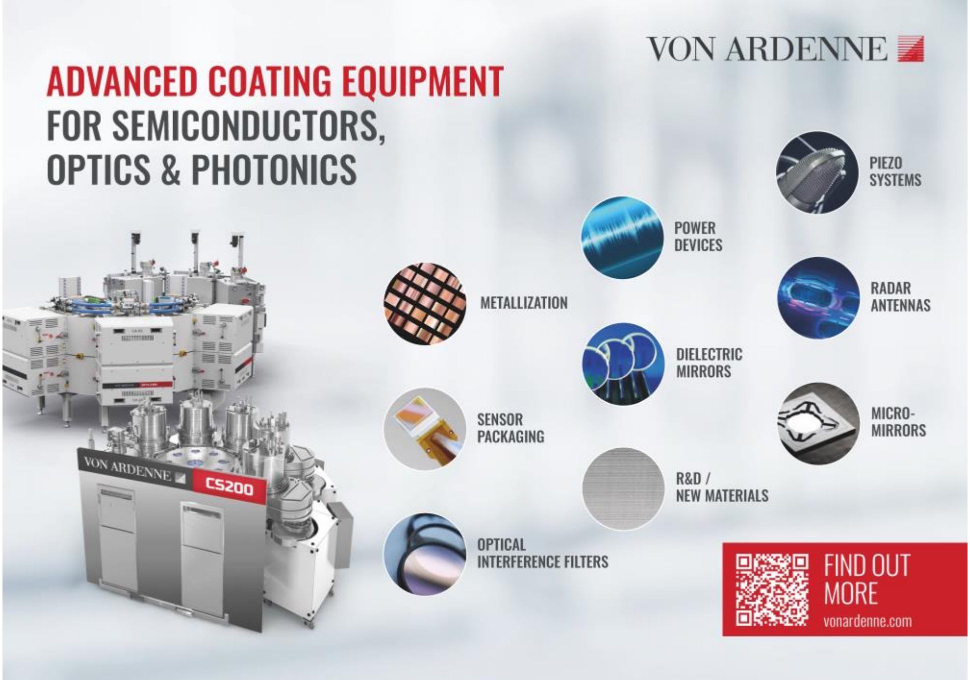
JX Advanced Metals

# GENERAL INFO

| | |
|---|---|
| FREE WIFI | Login: **Luxor public**<br>Password: **LUXOR911** |
| POSTER SCHEDULE | From Tuesday morning (March 24) to Wednesday (March 25) just after the afternoon coffee break |
| CONFERENCE DINNER | Wednesday 25 March • 18:30<br>**Ratsstube**<br>Johannisplatz 1,<br>09111 Chemnitz |



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# Key building blocks driving the developments of FD-SOI 10nm node

Claire Fenouillet-Beranger

*CEA-LETI, France*

In the context of 10 nm FD-SOI technology development, novel architectural features and process modules must be implemented to achieve the targeted device performance specifications. Strain engineering remains a key performance enabler and can be introduced either at the wafer level or locally at the device level. Additional process optimizations are required to further reduce access resistance and improve overall device characteristics. In particular, the integration of in situ doped, faceted raised source and drain regions is essential to minimize parasitic resistance. Meeting the aggressive contacted poly pitch (CPP) target of 68 nm requires the adoption of advanced patterning strategies, notably Self-Aligned Double Patterning (SADP), in order to satisfy density scaling constraints. This presentation highlights these technological levers and evaluates their impact on extending the performance capabilities of FD-SOI technology.

# From Full-Field to Single-Spot: Laser-Based Processing for Microelectronics

Clair, Maurice[a]

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The increasing complexity and miniaturization of semiconductor devices require innovative manufacturing solutions that deliver both high precision and thermal efficiency. This presentation examines a variety of laser processes for microelectronics, from full-field to single-spot processing, enabling next-generation microelectronics and encompassing applications from advanced diagnostics to power device and sensor fabrication.

By employing ultrafast lasers, systems such as 3D-Micromac's microPREP® achieve high-speed, athermal material ablation with micrometer-level accuracy (Fig. 1), significantly reducing preparation times from hours to minutes for complex semiconductor packages. Therefore, laser-based sample preparation is a versatile solution for failure analysis and quality control.

As an example of well-established processes in device fabrication, laser-based Ohmic contact formation (OCF) for Silicon Carbide (SiC) wafers is examined. Unlike traditional full-field thermal processing, localized UV-laser annealing delivers the precise energy density necessary for nickel silicide formation while minimizing global substrate heating (Fig. 1). This approach is essential for 3D integration and for maintaining the integrity of thin wafers especially in the field of power electronic device applications.

With selective laser-annealing, precision can be further enhanced. This technique is particularly suited for pinning magnetic reference layers in GMR and TMR (magnetoresistive) sensors. This targeted approach improves sensor performance and reliability while supporting sustainability by achieving substantial energy savings compared to global heating techniques.

Additionally, Laser-Lift-Off (LLO) and Laser-Induced-Forward-Transfer (LIFT) processes are discussed. These techniques illustrate the versatility of laser tools, enabling both pinpoint accuracy at the scale of microLEDs and large-area separation of functional layers, such as metal films, with high throughput.

The limits of miniaturization are extended through high-precision processing of electronic components at the 1-2 µm scale. Advanced systems such as 3D-Micromac's microVEGA FC facilitate the precise separation of individual fuses and electrical connections, combining exceptional accuracy with industrial-grade productivity.

In summary, laser-based processing provides a scalable, sustainable, and highly precise alternative to conventional thermal methods. Transitioning from large-scale treatments to targeted single-spot interventions, these technologies advance the development of high-performance microelectronics and next-generation power systems..

References

1. Use the Physical Review reference format
2. A. N. Example, Journ. Nam. **53**, 1256 (2007).

* *corresponding author e-mail: clair@3d-micromac.com*

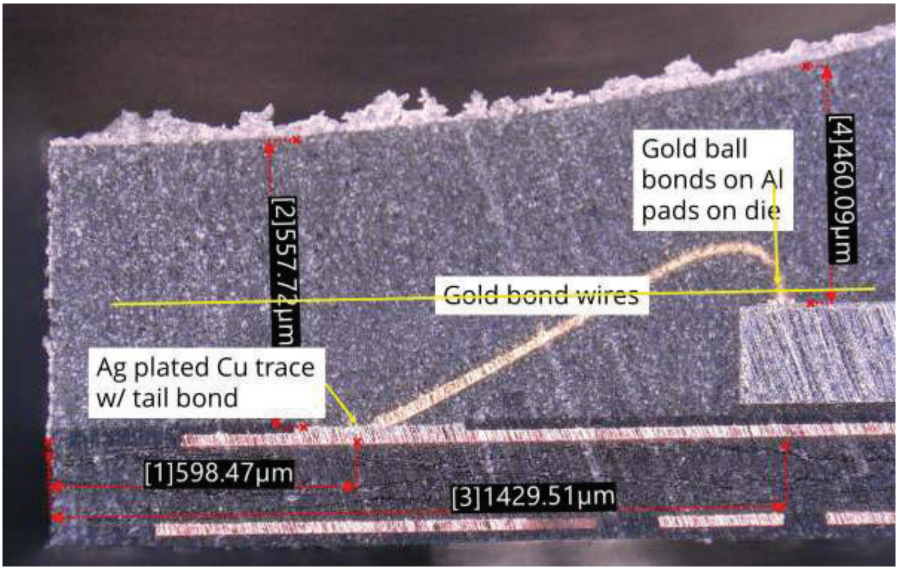

Figure 1: View of iBGA package-cross section prepared with ultrashort pulsed laser

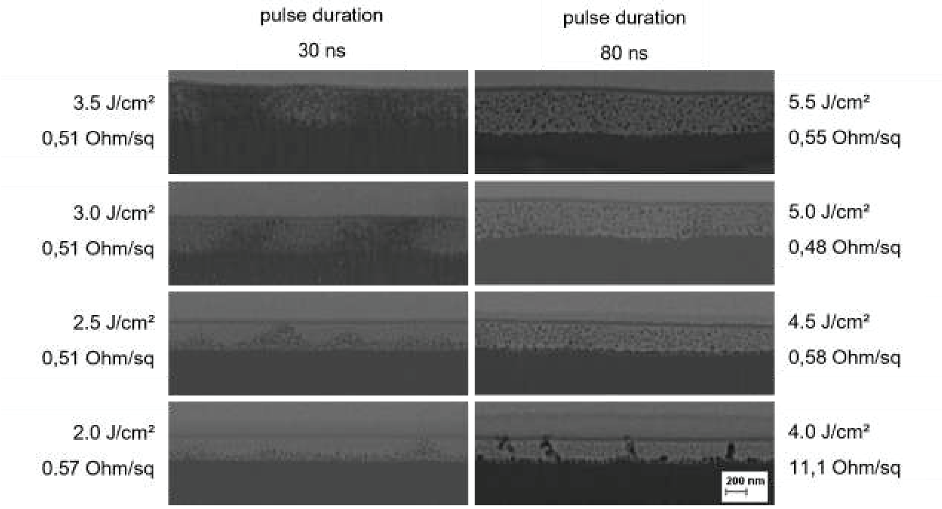

Figure 2: Comparison of $Ni_xSi_y$ interface formed by shorter pulsed laser and longer pulsed laser

# Chip-on-Wafer Integration Technology for Silicon Capacitor Embedded 3D Functional Interposer

Tatsuya Funaki[a,b] and Takayuki Ohba[a]

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[b] *Murata Manufacturing Co., Ltd., 1-10-1 Higashikotari, Nagaokakyo-shi, Kyoto 617-8555, Japan*

In case of the conventional 2.5D package, a large area for the capacitors is required and the wiring length from MPUs to the capacitors is long such as 5 mm. If capacitor chips are placed underneath MPUs, a shorter interconnect length between MPUs and the capacitors can be achieved. In our research, we have addressed barriers across multiple domains, including equipment and materials, to realize 3D integration technology for enhanced performance [1]. This paper describes Chip-on-Wafer (COW) integration applied to a miniaturized, capacitor-embedded 3D functional interposer.

The capacitor-embedded 3D functional interposer is fabricated by COW process on a 300 mm wafer, ensuring compatibility with Cu Damascene interconnect technology. COW process flow is shown in Fig. 1 [2]. The COW process mainly consists of three key technologies: (1) wafer warpage control utilizing waffle wafer, (2) narrow-gap chip bonding with a thin adhesive, and (3) TSV interconnects between capacitor and RDLs.

In this paper, wafer warpage control utilizing waffle wafer is focused. Wafer warpage, due to a mismatch in the CTE between Si and organic materials such as mold resin, causes wafer cracking and even wafer breakage in the worst case. To reduce wafer warpage, waffle wafer was introduced in the COW process. Waffle wafer can reduce the volume of mold resin, so wafer warpage is smaller than that of a mirror wafer.

By utilizing COW integration, capacitor embedded 3D functional interposer was demonstrated. Fig. 2 shows the parasitic capacitance as a function of interconnect length of TSV or line length for conventional 2.5 and new 3D functional interposer [3]. Since the interconnect length was reduced to less than 1/100, the parasitic capacitance was significantly reduced to 1/150 of that of conventional 2.5D. The capacitance measured in this study is as low as 50 ~ 100 fF, including TSV and RDLs. This extreme reduction of the parasitic capacitance is applicable for the low-voltage (Vdd) and lower-noise power supplies of MPUs. The COW-based capacitor-embedded 3D functional interposer demonstrated in this study integrates both capacitors and active devices, enabling further extension to high-density heterogeneous integration in advanced 2.5D/3D architectures.

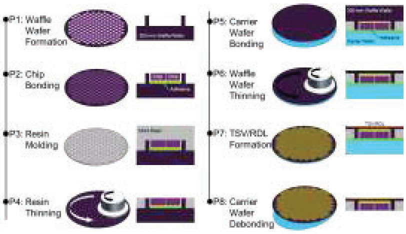

Fig. 1 Process flow for capacitor embedded 3D functional interposer are prepared using the bonding-first and TSV-last COW process.

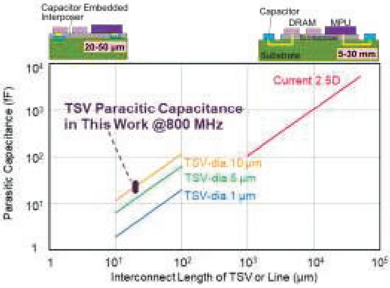

Fig. 2 Relationship between parasitic capacitance and interconnect length of TSV or line length. The interconnect length is over 5 mm in case of current 2.5D. In case that capacitor is placed underneath the active chip, the interconnect length is shortened to 20 µm.

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# Next-Generation Electrolytes for High-Precision Micro Bump Integration

Himendra Jha*, Jessica Stubbe, Christian Wendeln, Sandra Niemann, Ingomar Wolter, Recep Kocer

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The steady increase in interconnect density in advanced packaging continues to drive miniaturization of solder-based micro bump architectures. As pitch dimensions approach the lower limit of conventional three-layer pillar stacks, electrochemical deposition (ECD) processes must operate within increasingly narrow process windows. Reduced feature sizes intensify mass transport limitations, height variation sensitivity, and metallurgical interactions within confined volumes.

At these scales, uniformity is no longer solely a matter of wafer-level control but becomes a geometry-dependent challenge within complex hybrid bump layouts. Variations in pillar diameter, pitch, and local pattern density demand electrolyte systems capable of delivering geometry-independent deposition behavior while maintaining strict coplanarity and controlled vertical dimensions. Simultaneously, shrinking solder volumes amplify the impact of intermetallic compound formation and impurity-driven failure mechanisms, directly linking deposit chemistry to long-term reliability. As a result, electrolyte formulation evolves from a productivity parameter toward a central reliability driver in advanced packaging integration.

This work discusses the fundamental electrochemical and metallurgical constraints emerging in miniaturized micro bump technologies and outlines how tailored electrolyte design enables stable, high-uniformity deposition and controlled interfacial reactions within the solder-based regime. The results emphasize that further scaling of micro bump interconnects will depend not only on hardware innovation, but critically on chemistry-driven process optimization.

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# Hi-Temperature Lifetime Capability of CuAl Intermetallic Joints: Comparative Study of Pure and Alloyed Copper Wires through Electrical and Physical Methods

Alberto Mancaleoni[a], Gabriele Losacco[a], Roberta Carluccio[a], Riccardo Villa[a]

[a] *STMicroelectronics Srl, Via C. Olivetti 2 – 20864 Agrate Brianza (MB), ITALY*

In wire bonding interconnections, copper has replaced gold due to its cost and performance advantages, particularly when coupled with aluminum bond-pads. Alloyed copper wires can further improve reliability performance. This study investigates how the wire alloying elements can affect the time to wear-out of the Inter-Metallic Compounds (IMCs) between Cu wire and aluminum bond-pads when submitted to extended isothermal ageing (HTS). In previous work, a delaying effect of the alloying elements on the IMC evolution was observed through electrical resistance drift (Fig. 1a), but the ageing level reached was not sufficient to detect loss of integrity in the joint, which characterizes the wear-out stage. The investigation has therefore been continued through destructive Wire Pull Test (WPT) and inspection of cross-sectioned samples by SEM (Fig. 1b) and TEM to monitor the structural evolution of the joints in front of an extension of the HTS trials until 10000 equivalent hours at 150°C. IMC stoichiometry has also been studied on TEM lamellas through EDX tools (Fig. 1c) when the typical wear-out symptoms have been detected. The results confirmed the lifetime advantage hypothesized in the previous study for alloyed Cu, with a significant benefit for Hi-rel applications and aggressive geometry scale-down needing adoption of very thin wires. The electrical resistance drift, analyzed until the end of the experiment, did not provide evident signatures correlated with the physical wear-out observed in the joints, and this aspect may deserve further investigation. On the other hand, this non-destructive method has been demonstrated to be an effective early predictor of the lifetime potential if applied in a comparative approach between different materials. It can also be used to estimate the temperature acceleration factor of the degradation mechanism with an accuracy comparable to the rigorous method based on IMC thickness data, which requires a much higher experimental effort.

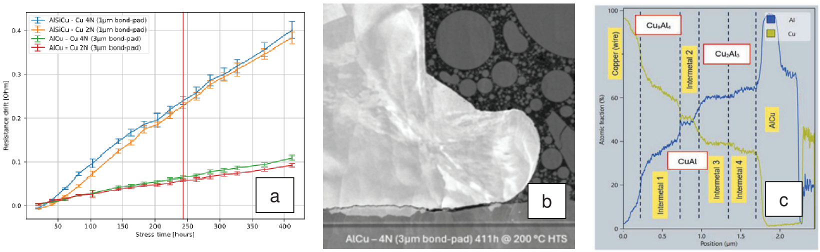

Fig. 1: a) Resistance drift plot, b) Aged bond cross section with IMC crack, c) IMC stoichiometry profile from TEM

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# Co-Registered Automated Optical Inspection and Metrology for C4/TCB Micro-Bumps with Infrared Structured Illumination Microscopy of Bonded Interfaces

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C4 flip-chip and thermo-compression bonding (TCB) interconnect schemes require the simultaneous control of micro-bump geometry (e.g. height, coplanarity, critical dimensions and deformation) and defectivity (e.g. missing/partial bumps, bridges, residues, damage and process excursions). Furthermore, advanced packaging process flows necessitate in-line measurements on both full wafers and chips on film frames, accompanied by robust automation and actionable statistics on substantial sample sizes. In practice, the separation of defect inspection and metrology frequently introduces registration uncertainty and limits correlation between defect appearance and quantitative geometry.

In this paper, we present a precision optical platform in which defect inspection and 3D/2D metrology share a single optical beam path, generating inherently co-registered datasets. The concept of "what you see" being aligned with "what you measure" by design is a fundamental principle that underpins the system. The system is based on Structured Illumination Microscopy (SIM) for quantitative topography and material-independent surface measurement, supporting nanometer-scale vertical sensitivity for demanding topographies such as micro-bumps and high-aspect-ratio features [1,2]. In the context of micro-bump AOI, high-resolution imaging is combined with AI-driven workflows (e.g., classification/segmentation/anomaly detection) to minimize false positives and enhance decision-making for process optimization [3].

A key enabler for information-rich micro-bump analytics is high sampling density. With an effective pixel size down to 0.55 µm at 10× magnification, the acquired data density is 3× higher per unit area compared with respect to state-of-the-art tools. This enables more robust bump-shape descriptors, tighter coplanarity statistics, and improved sensitivity to outliers in large populations. The platform has been engineered to measure hundreds of millions of bumps per wafer, perform automated statistical analysis, and flag defective bumps while delivering both defect review imagery and full-wafer image outputs.

In the context of wafer bonding, infrared is utilised for the specific purpose of inspecting and metrology of bond-interface. The present study proposes an extension of SIM into the infrared domain through the implementation of Infrared Structured Illumination Microscopy (IR-SIM), a technique that integrates the penetration of infrared light through silicon with the optical sectioning of samples [4]. The method projects sinusoidal illumination patterns, acquires two phase-shifted images, and demodulates them to suppress out-of-focus contributions. This enables depth-resolved "optical cross-sectioning" and quantitative 3D reconstruction at the buried bonding plane. The demonstration is conducted on Si–Si bonded wafers, utilising IR-SIM imaging to visualise voids, delamination, and bonding non-uniformities at the interface. This approach affords true 3D morphology with sub-micrometre resolution while maintaining non-contact operation and eliminating the need for sample preparation.

Beyond micro-bumps and bond interfaces, the same measurement concept supports additional advanced-packaging metrology tasks such as depth, profile, and CD measurements of dicing trenches and TSVs, wafer warpage, and total thickness variation (TTV). These tasks are enabled by the platform’s multi-sensor capabilities.

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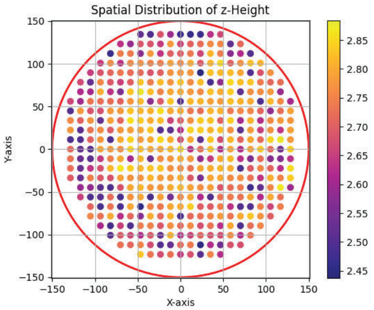

Figure 1: *Colour-coded 300 mm wafer map of the height distribution of the bumps.*

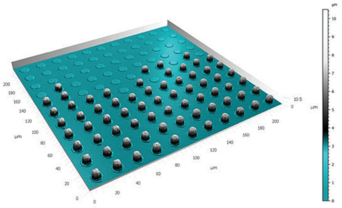

Figure 2: *3D rendering of an area with multiple missing bumps.*

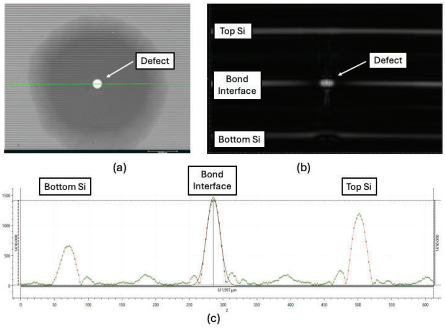

Figure 3: *(a) IR SIM top view of a defect and void at the Si-Si bond interface. (b) Cross-sectioning view of bonded Si wafers with a defect at the interface. (c) Pixel view of the wafer stack. The 3 peaks correspond to the Air-Si transition of the bottom wafer, bond interface, and Si-Air transition of the top wafer from left to right.*

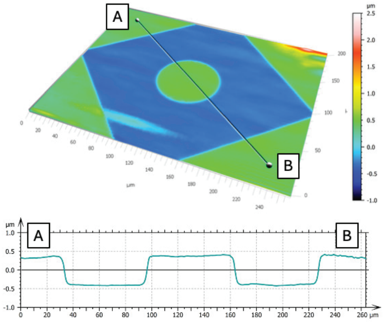

Figure 4: *(Top) 3D rendering of a square cavity with a round pillar at the bonding interface of 2 silicon wafers. (Bottom) 2D measurement of the cavity and pillar along the line A-B.*

# Benefit of post etch treatment for defectivity improvement in the BEOL

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In the challenging context of backend integration, the trench first hard mask architecture demonstrated its interest as the cost efficient solution for volume manufacturing as well as the time effective solution for yield learning. However, one major challenge using such integration is the metal fluoride crystal formation after etching leading to line and via opens.

The mechanism of residue formation is attributed to fluorine species reacting with titanium nitride and being catalyzed by air moisture. More precisely, fluorine and air moisture react to form HF compounds, which react with the TiN to form metallic salts [1].

The impact of the etch chemistry on metal crystal growth as a function of the air exposure time is presented in Fig.1. Important residues are observed only after 2h air exposure when blanket TiN wafer is exposed to high polymerising fluorocarbon chemistry as main or last step. However, when using low polymerising fluorocarbon (FC) chemistry some residues are observed after 8h. This result clearly underlines the impact of the etch chemistry on the metal crystal growth. This is related to important fluorine reduction at the TiN surface (-35%) when using low FC chemsitry compared to high FC chemistry (XPS analyses).

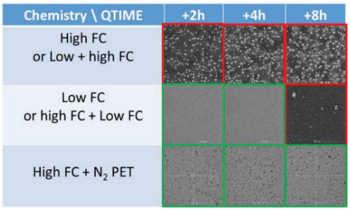

Fig. 1 : TiN surface observation by CD SEM after exposure to different etch chemistries/combination and $N_2$ Post etch treatment

Fig. 1 also shows that $N_2$ PET addition after high polymerising chemistry strongly reduces the formation of residues as a function of air exposure time. No residues are observed after 8h air exposure. This result is confirmed with XPS analyses showing that $N_2$ PET reduces the fluorine concentration from 31% to 25% at the TiN surface. The $N_2$ PET impact on TiN surface is to reduce fluorine at the surface limiting the reaction (F + air moisture) responsible of metal crystals formation.

Therefore, the choice of the last etch chemistry step seen by the metal hard mask is key to limit metal crystal formation. The use of a low polymerising chemistry as last step is strongly recommanded. Adding an in-situ post etch treatment like $N_2$, after etching, is essential too. It helps to reduce the fluorine concentration at the TiN surface (and therefore reduce the risk of metal crystal) but we will also demonstrate that $N_2$ PET is mandatory to passivate the copper surface avoiding other kind of defectivity like copper extrusion.

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# Multilayer $PtCoO_2$ Delafossite thin films for future interconnect metallization

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Advancing logic and memory technologies requires ever-smaller interconnects, now nearing 10 nm, where conventional Cu wiring suffers from severe performance and reliability limits. While early research explored refractory metals as Cu alternatives, growing interest now centers on binary and especially ternary intermetallic compounds that may offer superior properties [1,2]. Because the ternary design space is vast, current efforts focus on targeted families such as MAX phases and delafossites to identify promising next-generation interconnect materials.

Delafossite oxides like $PtCoO_2$ and $PdCoO_2$ exhibit extremely low in-plane resistivity and long mean free paths, but thin-film versions still fall far short of single-crystal performance due to crystallinity issues such as twin domains, impurity phases, and substrate mismatch [3,4]. These advances demonstrate that careful interface engineering and precise oxygen control are essential for achieving high-quality, low-resistivity $PtCoO_2$ thin films.

Our work shows that epitaxial $PtCoO_2$ thin films can achieve outstanding electrical performance at nanoscale thicknesses. Through optimized substrate conditioning, controlled oxygen incorporation, and multilayer deposition, the films show high crystallinity with narrow full width at half maximum of 0.22° for 16nm thick film (and good epitaxial relationship as shown in Fig.(a) and (b)). $PtCoO_2$ films attain low resistivity (4.7 µΩcm at 16.3 nm thick film obtained using a three-layer $PtCoO_2$ approach, in Fig.(c)), and reduced defect levels (below 0.5% for void density). This firmly positions $PtCoO_2$ as a contender for future interconnect applications. While additional studies on interfacial chemistry and long-term reliability are still needed, these results outline a clear route toward leveraging delafossite oxides in advanced interconnects, with future efforts aimed at scaling the process for industrial use and integrating it into existing BEOL platforms, probably by layer transfer as demonstrated recently for the epitaxial Ru [5].

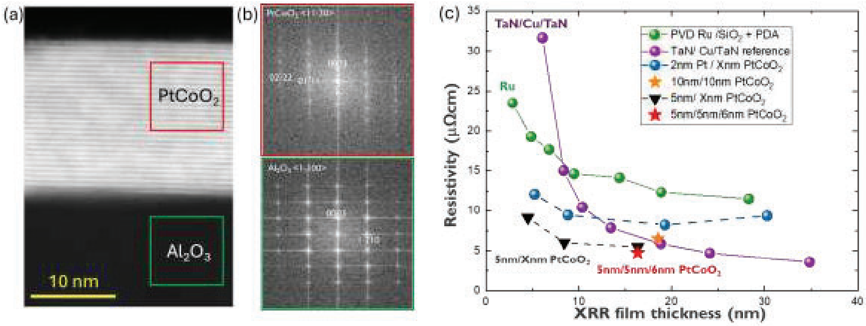

Figure (a): Cross-TEM of 5PCO/15PCo stack. (b) FFT of the PCO and the c-plane $Al_2O_3$ sapphire showing the epitaxial relationship. (c) Resistivity of different flavors of epitaxial $PtCoO_2$ deposited on c-sapphire.

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# Ruthenium Based BEOL Integration Schemes for Scaled Interconnects

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Reducing interconnect resistance and capacitance remains essential to sustain performance as BEOL scaling enters the sub-20 nm metal-pitch regime, where RC delay, variability, and integration complexity rapidly increase [1]. Direct-metal-etch ruthenium (Ru) [2-5] has emerged as the leading candidate replace copper (Cu) for the most scaled metal levels, owing to barrier-less integration, limited resistivity degradation at reduced dimensions, and superior electromigration robustness. In parallel, process options such as fully self-aligned vias (FSAV) and air-gap structures are proving effective at lowering capacitance and mitigating via-to-line leakage [4, 5].

In this invited talk, we present imec's BEOL roadmap direction and the Dual Direct Metal Etch (DDMe) [1] integration approach. DDMe enables multi-layer FSAV through direct etching of both line and via levels, removes conventional barrier/liner stacks in vias and it is highly compatible with air-gap integration. Recognizing that Cu will remain essential in upper metal levels, we also focus on on Cu/Ru co-integration. Using stacked-via resistance modelling and experiments on selective Ru (Vias) on Cu (wires) via in EUV-patterned dual-damascene levels, we show that hybrid Ru-via/Cu-wire schemes bring substantial performance benefits even though more work is needed on the integration approach compatible with DDMe [9]. Collectively, DDMe and hybrid Ru/Cu metallization constitute a flexible, manufacturable platform to address near-term RC and variability constraints while keeping optionality for future conductors and heterogeneous BEOL stacks [10, 11].

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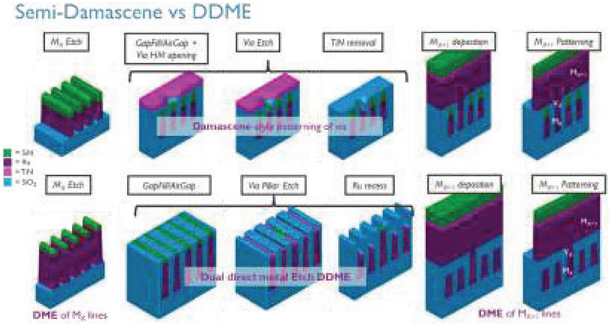

# Wafer level technologies for Heterointegration of Photonics Modules

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Silicon Photonics is a key technology for Photonics / Electronics convergence. Today, increasing bandwidth needed in data center interconnects drive the deployment of silicon based advanced modules, e.g. Co-packaged Optics modules (CPO). This new paradigm strongly relies on advanced packaging technologies initially developed for memories or high-end CPUs. These wafer level technologies, such as TSVs, fine pitch interconnects of Fanout Wafer Level Packaging (FOWLP), are currently being applied to Photonic Integrated Circuits (PICs) to cope with the emerging needs, enabling volume manufacturing of high speed photonic transceivers [1].
In this presentation, we will review recent requirements related to CPOs and integrated process flows developed at CEA-LETI in order to apply such advanced packaging technologies to PIC, in various applications fields such as Optical Phased arrays (OPAs) for LIDARs, and Optical Network On Chip (ONoC) based photonic interposers for High Performance Computing (HPC).

First development has been led in order to build multi processors ONoCs. For this purpose, we developed a full integrated flow enabling TSV and wiring formation on PICs [2]. We investigated the potential influence of TSV close to optical features (such as waveguides or Ring Resonators). In some cases, influence of TSV due to mechanical stress can be observed, especially on phase-based devices (e.g. Mach Zehnder interferometers) [3]. These measurements led to establish design rules, particularly Keep Out Zones (KOZ) for future designs of complex interposers.

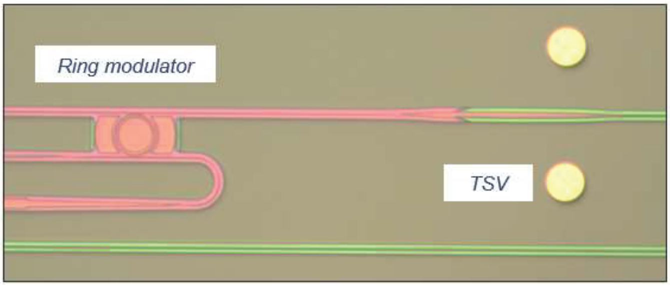

Fig 1 Top view of a photonic interposer with Ring Resonator Modulators and TSVs.

Figure 1 shows a picture of photonic circuitry integrated with TSV-mid features, used to demonstrate Optical Network On chip combining CMOS manycores chiplets, Electronic IC (EIC) dedicated to photonic devices driving and thermal management, both being flip-chip assembled on a large PIC interposer using 40µm pitch copper pillars. In [4] we recently demonstrated for the first time such an architecture with dynamic routing between chiplets, achieving the lowest published latency for a reach of around 2.5cm, while being capable of longer reach on interposer and extension to other dies through optical fiber.

In another development, we applied this mid process TSV integrated flow to OPA, in order to perform beam steering for LIDARs. Traditional wire bonding technologies lead to chips that are too large, due to the number of electrical functions to be wired, in particular the heaters used as phase shifters in the OPA. By applying our process to OPA-type photonic chips, we obtained functional demonstrators, a cross-section of which is shown in Figure 2.

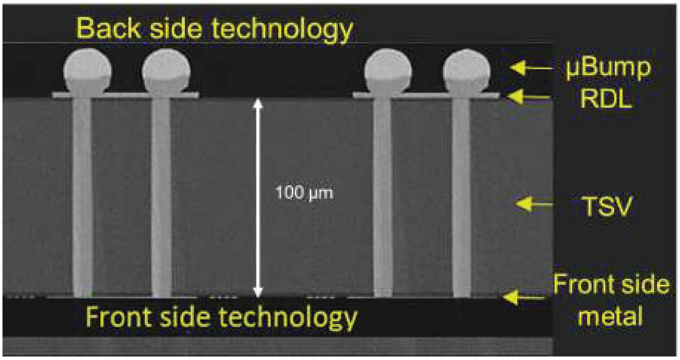

Fig 2 : Lidar OPA built using mid process TSV integration to enable back side interconnections

In this work, obtained within the TINKER European project (H2020), we performed the complete functional demonstration of our functional device, including TSV formation, chip thinning, flip-chip bonding, PCB integration and fiber pigtailing [5]. A motherboard to control the 256 channels heating, the 1550 nm laser and its power supply as well as a temperature monitoring unit have been installed in the demonstrator body and a specific software has been developed to control the different parameters of the system and generate the beam steering scenarios for the characterizations and the real time demonstration. This demonstration confirmed the validity of this approach in term of form factor and potential for collective manufacturing using standard microelectronic processes.

In order to address the requirements of coming CPO modules, several challenges remain. Among them, it is needed to develop detachable connectors to connect the PIC to external fiber optics bundles. Legacy technologies such as conventional assembly of Fiber Array Units are limited in terms of fabrication throughput and reliability. Alternative solutions rely on lensed optical schemes, relaxing the assembly tolerances of lensed connector versus lensed PICs. In this case, the placement of lenses towards PICs and fiber need to be carefully controlled. We developed several approaches, including use of self-assembly techniques relying on solder melting [6] or greyscale lithography [7].

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# How wafer direct bonding mechanism enables die-to-wafer technology.

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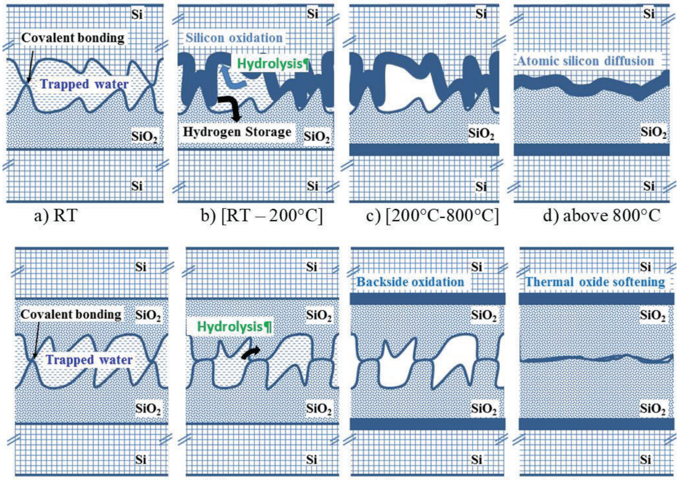
Direct bonding, of which hydrophilic molecular bonding is now the most widespread type, is currently used in mass production in the microelectronics industry. After a brief introduction to direct bonding, we will focus on this specific subtype. We will analyse the origin of its adhesion energy, which enables the bonding to self-propagate, as well as the consequences in terms of defectivity when the Joule–Thomson coefficient of the bonding atmosphere is positive.

After bonding, although covalent bonds are already present at room temperature, adherence generally remains weak. A thermal annealing step is therefore required to increase the density of these bonds until complete sealing of the interface is achieved. To shed light on the physicochemical mechanisms responsible for this increase in adherence using silicon dioxide material (cf. Fig. *1*), we will briefly discuss results obtained from other types of direct bonding. This comparison will highlight the central role of interfacial water and its influence on the mechanics of silica asperities. In particular, we will see that chemical catalysts can be used to drastically enhance adherence at low annealing temperatures (cf. Fig. *2*). These chemical bonding energy boosters can replace the standard plasma treatment to obtain plasma free direct bonding.



a) RT b) [RT – 200°C] c) [200°C-800°C] d) above 800°C

e) RT f) [RT – 600°C] g) [600°C-1200°C] h) above 1200°C

Fig. 1 : Mechanism for silicon and silicon dioxide molecular direct bonding [*1*].

Of course, changing the bonded material will drastically impact the bonding mechanism to explain the adherence evolution. Usually, the adhesion energy and the direct bonding propagation is not impacted by the bonded material. As an example, copper/copper bonding mechanism will be discussed. This opens the way to hybrid bonding as this bonding uses two hybrid surfaces made of copper and $SiO_2$.

Wafer-to-wafer bonding, using wafer diameter up to 300mm, presents many advantages in terms of large bonded area, availability of advanced CMOS wafer and compatibility to any microelectronic classical process. However, many materials of interest, such as InP and GaAs, which are commonly used in photonic applications, are not available in large wafer sizes. Moreover, in 3D applications, the bottom and top chips do not have, in general, the same sizes. And even if they have the same size, it is highly advantageous for overall yield to bond only functional chips onto functional chips. This approach cannot be implemented using wafer-to-wafer bonding.

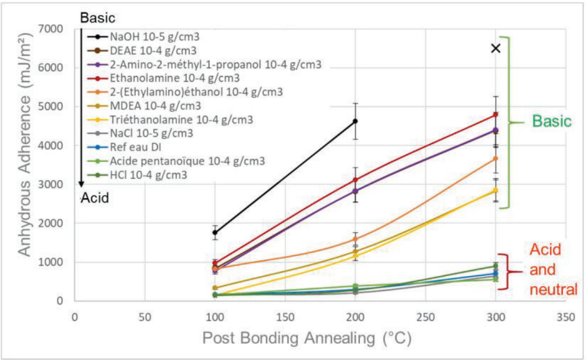
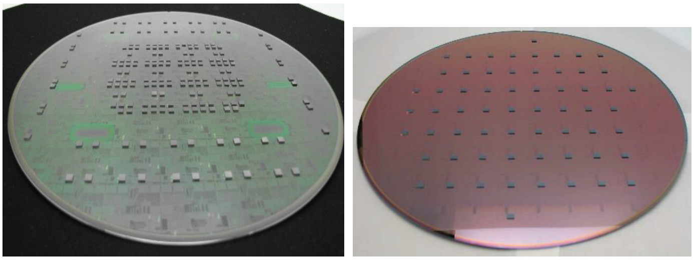


Fig. 2 : Chemical bonding energy boosters for $SiO_2$//$SiO_2$ direct bonding [2].

Die-to-wafer bonding, which maintains the advantages of a direct bonding interface, offers significant potential for integrating different materials or enabling pre-bond functional testing of dies. Even if the fundamental direct bonding mechanisms are not changed, some specific features have to be taken into account for die bonding. For instance, edge effects during and after the bonding or annealing, significantly impact both bonding energy and interface defectivity. To reduce interface defectivity, a specific bonding technique using liquid water could be employed only in die-to-wafer bonding. If all these specific features are under control, then, very innovative structures could be obtained. It is possible for instance to bond small 3 mm*3 mm InP dies onto a 200 mm silicon photonic wafers as shown on Fig. 3a [3]. Moreover, hybrid bonding interface could be also obtained between 6 mm*4 mm dies and a 300 mm wafer as shown on Fig. 3b. For hybrid bonding, precise alignment is mandatory. This can be achieved using die-to-wafer bonder, but innovative technologies such as capillary-assisted self-assembly could also be highly beneficial [4,5].



a) b)

Fig. 3 : a) *InP dies directly bonded on a photonic SOI wafer. b) Die-to-wafer hybrid bonding example.*

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# Ti metallization for p-GaAsSb base contact

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Antimony Sb-based optoelectronic devices have recently attracted significant attention for their potential in lower-power, high speed electronic applications [1][2]. Among these, InP/GaAsSb double-heterojunction bipolar transistors DHBTs stand out as particularly the most interesting devices. Designed to overcome the electron blocking effect commonly observed at the base-collector heterojunction of type- I InGaAs- based DHBTs [3], these InP/GaAsSb- based type- II devices offer improved carrier transport and enhanced breakdown characteristics [4]. As a result, they have emerged as strong candidates for terahertz (THz) integrated circuit applications, achieving maximum oscillation frequencies $f_{max}$ exceeding 1.2 THz and common-emitter breakdown voltages greater than 5.4 V.

GaAsSb layers are often metallized using noble metal such as gold, palladium, or platinum [5]. While unreacted stacks based on these metals can provide very low specific contact resistivity $\rho_c$, typically between $10^{-6}$ and $10^{-8}$ ohm.cm$^2$, they are incompatible with standard silicon fabrication lines, making them unsuitable for CMOS-compatible processes. Recently, significant progress has been made in this direction through the development of a fully CMOS compatible contact technology [6]. Alternatively, titanium (Ti) has been shown to achieve similarly low $\rho_c$ values when deposited directly on p-GaAsSb. Its CMOS compatibility makes Ti a promising candidate for integrating III-V layers with silicon, combining low-resistance contacts with process compatibility [7]. This work spans all critical stages, including surface preparation, solid-state reaction analysis, electrical characterization, and integration strategy development, ensuring compatibility with advanced industrial processes.

The experimental protocol consists of a metallization process carried out for physicochemical characterization and the fabrication of TLM. The metallization schemes investigated in this work were based on Ti 10 nm/TiN 8 nm multilayer structures, with Ti serving both as an adhesion layer and the primary ohmic contact with the semiconductor. TiN diffusion barrier layer was used to limit interactions with ambient air. For each sample annealed with a 60 seconds RTA under $N_2$, average values of specific contact resistivity are shown in figure. 1.a The as-deposited sample exhibits a specific contact resistivity of $\rho_c = 1.4 \times 10^{-4}$ ohm.cm², which decreases to a minimum of $\rho_c = 2.6 \times 10^{-5}$ ohm.cm$^2$ after RTA at 350 °C, indicating improved ohmic contact quality. The contact resistivity remains stable up to 400 °C suggesting good thermal stability and preserved semiconductor integrity, with no significant metal diffusion or contamination. Standard deviation of $\rho_c$ decreases significantly with temperature increasing. Beyond 400 °C a sharp increase in resistivity is observed, reaching $\rho_c = 2.3 \times 10^{-2}$ ohm.cm$^2$ at 500 °C, indicating a loss of ohmic behavior likely caused by metal diffusion and the formation of interfacial compounds.

In order to further improve $\rho_c$ for the lift-off flow, an additional thermal treatment was performed in two successive steps: 60 seconds at 250°C, followed by 60 seconds at either 450°C or 500°C. The results in figure 1.b shows that two successive annealing steps allows that Ti (10nm) / TiN (8nm) stack remains stable up to 450 °C, with a specific contact resistivity optimized at $\rho_c = 2 \times 10^{-5}$ ohm.cm$^2$. Beyond this temperature, irreversible degradations occur, affecting both the metal interfaces and the semiconductor.

To further investigate these Ti-based contacts, ToFSIMS analysis was performed on the TiN/Ti/GaAsSb system right after metal deposition and after annealing at 300 °C, 400°C and 500°C (see Fig. 2). The measurements were conducted in positive polarity to effectively monitor the system evolution. A clear interface is observed without annealing between Ti and GaAsSb layers even if oxygen signal shows a low intensity due to native oxide presence on the top of III/V surface before the metal deposition. After 300°C annealing, Ga element begins to diffuse in Ti layer leading to the onset of $TiGa_x$ intermetallic alloy formation at the Ti/GaAsSb interface. At 400°C, the Ti layer becomes significantly thinner while $TiGa_x$ grows, evidencing a stronger reaction at the interface. At 500°C, the Ti layer is almost fully consumed, and a mixed region containing Ti, As, and Sb is detected at Ti /GaAsSb interface, confirming advanced chemical reactions between the metal and the semiconductor.

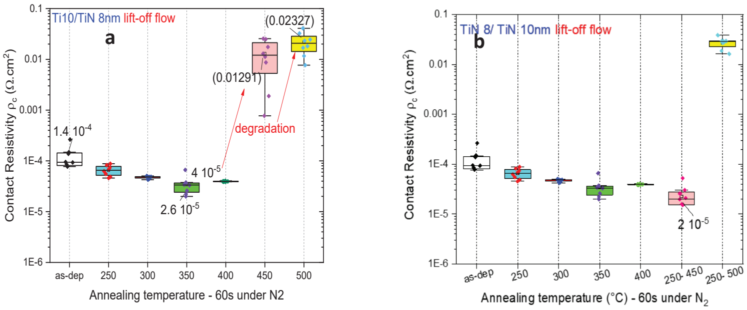

***Fig. 1 .a .b –** Specific contact resistivity of the Ti (10nm) / TiN (8 nm) stack on carbon-doped GaAsSb as a function of temperature .*

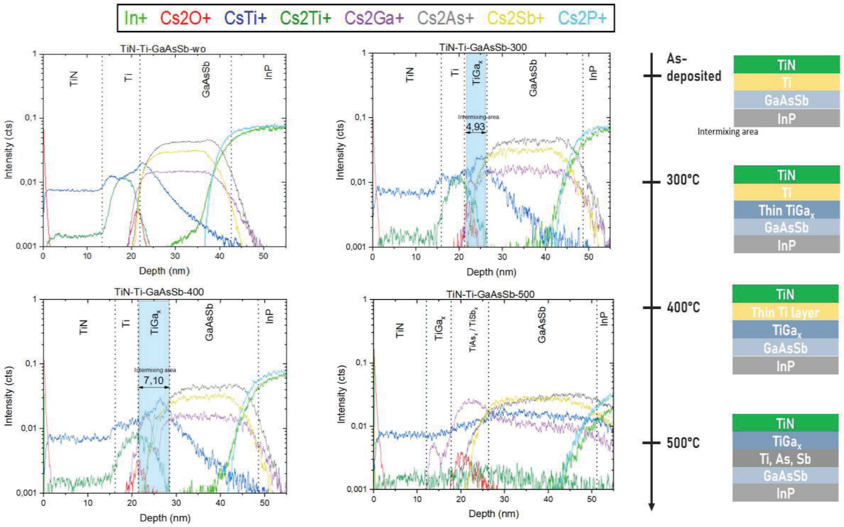

**Fig.2 –** T*oFSIMS profiles of the TiN/Ti/GaAsSb system annealed at various RTA*

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# Bond Front Kinetics and Adherence of Direct Wafer Bonding in Dielectric-Dielectric Interfaces

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Direct wafer bonding of dielectric materials is a cornerstone of 3D integration and a precursor to fine-pitch hybrid bonding [1]. While dielectric-to-dielectric fusion provides the necessary mechanical stability and hermetic sealing for heterogeneous integration, the underlying physical and chemical mechanisms governing bond front propagation and post-bond adherence energy remain insufficiently understood. This study systematically investigates these dynamics across various PECVD films, including $SiO_2$, SiON, and TEOS $SiO_2$, to establish a predictive framework for optimizing surface kinetics and bond strength in next-generation interconnect architectures.

All dielectric layers were deposited via PECVD on 150 mm Si wafers with a nominal thickness of 500-570 nm. Following Chemical Mechanical Polishing (CMP), all surfaces achieved a root-mean-square (RMS) roughness below 0.25 nm to ensure spontaneous bonding [2]. The room-temperature bonding process was captured via infrared (IR) camera under monitored ambient conditions. The impact of surface pre-treatments, such as DIW rinse, a standard RCA cleaning, and plasma activations, such as $N_2$ + DIW rinse, $O_2$ + DIW rinse and Ar + DIW rinse was also studied. An AI-based algorithm was employed to extract the bonding speed from the IR footage. Finally, the resulting adherence energy was quantified through Maszara's blade insertion method [3] [4].

These findings provide a high-resolution benchmark for selecting dielectric-activation pairings tailored to specific integration requirements. Ongoing work focuses on the development of multi-physics models to correlate these experimental kinetic data with simulated surface energy and stress distributions. These modeling efforts aim to provide a predictive tool for optimizing bond uniformity and interface integrity in next-generation high-density 3D integration technologies.

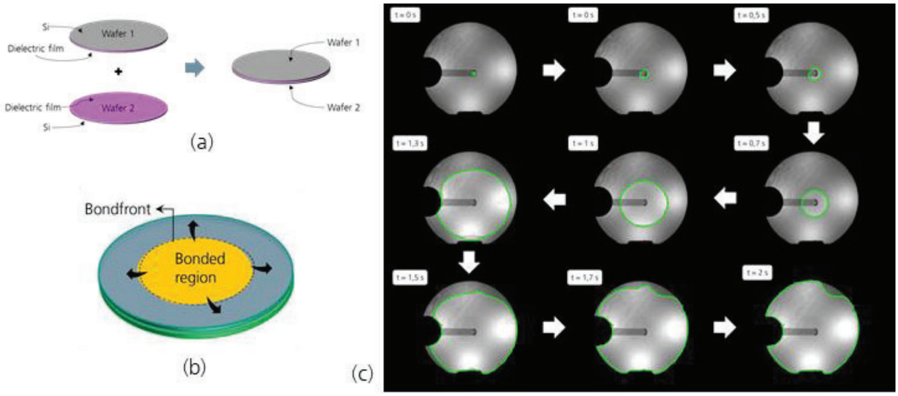

Figure: (a) A schematic showing dielectric to dielectric direct wafer bonding; (b) A schematic showing bond front during bond front propagation; (c) A sequence of images showing bond front propagation (green annotation for bond front) with time stamps

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# Shear tests of BEoL interfaces with in-situ SEM imaging

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The need for measuring or ranking the adhesion between thin dielectric caps (< 50nm) and metal layers is part of the failure mode and effect analysis to be addressed when developing new Back-End of Line (BEoL) stacks. The mechanical test suitable to compare different interfaces should both be capable to promote the failure mode of interest and provide a figure of merit sensitive to the differences in adhesion energy and/or interfacial strength. Testing dedicated structures directly on the true device is also a relevant added value, when there exists a perspective to include such characterization into automated quality control.
In this view, the shear test was identified as an eligible test method: this consists in pushing a flat-faced chisel against the free edge of a test structure (from now on, the *button*), the latter constrained at the interface of interest. The test ends when the button no longer offers lateral reaction to the movement of the chisel and the typical figure of merit is the maximum lateral load achieved during the test (from now on, the *critical load*).

The shear test is very common in the qualification flow of packaging and wire-bonded interfaces [1], where the surfaces exposed on both the substrate- and the button-side suit the qualitative assessment of the failure mode. Implementing the test in the framework of BEoL stacks poses additional challenges, owed to the smaller characteristic length scale of the layers of interest [2]: in this work, the presence by design of a thicker dielectric (Silicon nitride, SiN, 500nm) on the thin dielectric cap was exploited to mill prismatic test structures using Gallium focused ion beam (FIB); test structures were milled targeting an in-plane footprint visible at an optical microscope (10x10µm), enabling relocation and successful shear tests of two Copper (Cu) / cap interfaces, using a bi-directional nanoindentation device (Hysitron TI-980, Bruker). Noteworthy, the interfaces under comparison not only featured measurable differences in the critical load, but also in the shape of the softening branches past the critical load.

While testing on standalone nanoindentation platforms is convenient in the view of potential automation and increased throughput, the assessment of failure modes relies on ex-situ observation methods, lacking deep insights into the origins of different kind of failures. For this reason, measurements were repeated using a compact nanoindenter (ZHN/SEM, Asmec) meant for installation in Scanning Electron Microscopes (SEM): a deep trench was FIB-milled on one side of the button, enabling in-situ SEM imaging during the shear test; the sequence of images revealed a markedly different extent of Cu plastic deformation for the two interfaces under comparison, suggesting a correlation between the extent of Cu plasticity before complete button shear off and the shape of the softening branches previously observed in the experimental campaign with the standalone indenter. Noteworthy, the assessment of the failure mode (*interfacial delamination* versus *cohesive Cu failure*) was itself not trivial and required relocation and transfer of the sheared button into a SEM equipped with a detector for Auger Electron Spectroscopy (AES), for shallow-depth analysis of the chemical content of the button surface exposed by the test.

In summary, this work illustrates the implementation of a shear test meant to compare Cu/cap interfaces relevant for BEoL stacks. In-situ SEM imaging is proposed as a suitable mean to gain insights in the physics of failure. These additional information enabled a more comprehensive interpretation of the load trends already accessible with standalone platforms, which in turns potentially suit automated and extensive experimental campaigns.

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# Reactive diffusion in Ni-Co-Si Ternary system using Bilayer and Alloyed thin films

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From 5G to automotive technologies, next-generation microelectronic circuits hinge on high-performance nanometric MOS transistors. Metal silicides are essential in CMOS technology as contacts for source, drain, and gate regions, reducing resistivity and enhancing device efficiency. These contacts are obtained by solid-state reaction between a metal film and the Si substrate [1]. $TiSi_2$ and $CoSi_2$ were widely used contacts but exhibited resistivity issues at submicron dimensions. In contrast, NiSi, although having a line-width-independent formation, suffers from poor thermal stability due to its transformation into $NiSi_2$ above 700 °C or to agglomeration at temperatures as low as 500°C for very thin films. To overcome these drawbacks, alloyed silicides are being investigated to improve the formation and stability of the silicides [2,3]. This study focuses on the phase formation kinetics in Co silicide alloys for the Ni-Co-Si systems. The effect of Ni on the phase evolution and the kinetics of silicide formation by reactive diffusion is investigated using in situ techniques and simulations.

Bilayer thin films with varying Ni and Co thicknesses, as well as the corresponding alloy thin films (Figure 1), were thermally annealed under different conditions to study the sequences of phases and kinetics of phase formation. After cleaning the silicon substrate with HF, Co and Ni bilayer and alloy films with varying Ni compositions (25%, 50%, and 75%) were deposited using magnetron sputtering from Co and Ni targets. In situ X-ray diffraction (XRD) was employed to observe the real-time phase evolution during step annealing at increasing temperatures, complemented by isothermal XRD annealing for detailed analysis of phase transitions and kinetics. In situ sheet resistance measurements were also conducted using a four-probe method to observe the changes in phase formation as well as the electrical properties of the silicides as they formed.

The main phases observed are the metal-rich phase $(Co1\text{-}xNix)_2Si$, the two monosilicides based on CoSi and NiSi, and the silicon-rich phase $(Co_{1-x}Ni_x)Si_2$. (Figure 2). The XRD results indicate that nickel significantly accelerates the formation of $M_2Si$, MSi, and $MSi_2$ silicide phases (M indicates the $Co_{1-x}Ni_x$ mixture of Ni and Co). Growth kinetics of the phases are increased by the composition of Ni, as Ni is the fastest diffusing species. The formation temperature of the $M_2Si$, MSi, and $MSi_2$ phases reduces as the concentration of Ni increases (Fig. 3). In bilayer films, the simultaneous formation of NiSi and CoSi phases was observed, especially when the Ni concentration exceeded 25%. However, there is no formation of NiSi observed for 25% Ni in the sample, which is due to the solubility limit of Ni in the metal sublattice. These results can be described using the ternary phase diagram (Fig. 4). The simulations using a reaction/diffusion-controlled growth model of the in situ XRD measurements allowed us to determine the growth kinetic parameter of the $M_2Si$ phase. For increasing Ni concentration, the activation energy for diffusion shows a decreasing trend, indicating a reduction in the kinetic barrier for diffusion. In situ sheet resistance measurements show that increasing the Ni concentration shifts the transition from high to low sheet resistance to a lower formation temperature of the phases (Fig. 5). This indicates that the Nickel in the film influences the phase formation kinetics of the phases and the resistivity changes accordingly. This research gives valuable insights into silicide formation mechanisms and their impact on device performance, contributing to a new path for optimizing contact materials in advanced microelectronic circuits.

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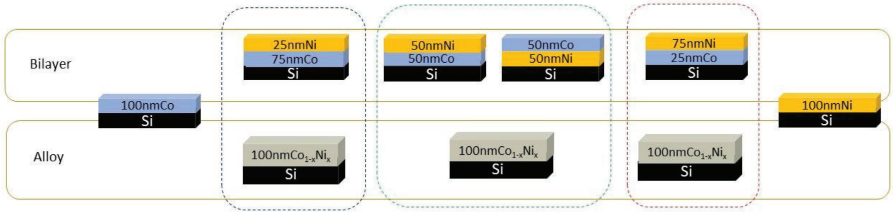

Figure1. Schematic representation of samples analyzed

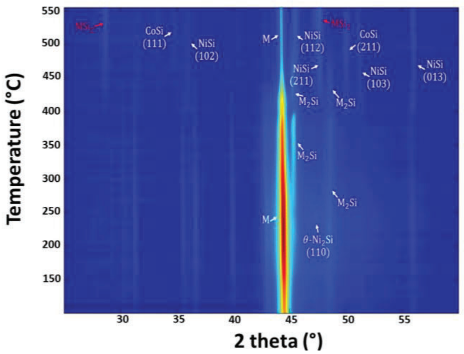

Figure 2. In situ XRD patterns for the bilayer sample 50nmNi/50nmCo/Si

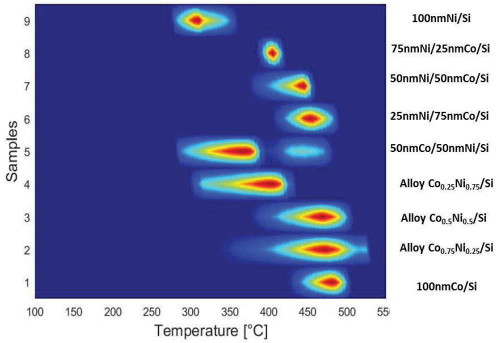

Figure 3. Comparative kinetics of the M2Si phase in the different samples

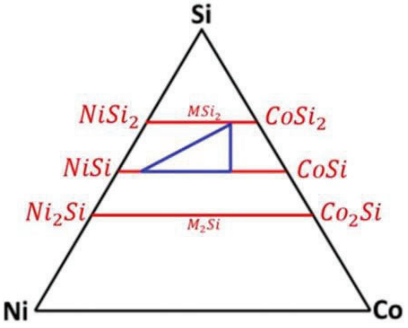

Figure 4. Calculated Co-Ni-Si ternary phase diagram at 400°C for thin film reaction. The equilibrium between CoSi, NiSi, and MSi2 is drawn in blue

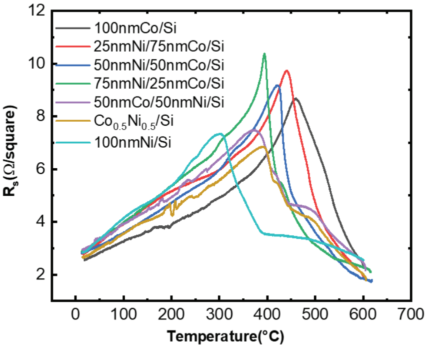

Figure 5. In situ Sheet resistance as a function of Temperature of the Ni-Co-Si samples

# The formation mechanism and kinetics of $Ni_3GaAs$ nano-thin films on GaAs

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III-V semiconductors, particularly GaAs, are of great interest due to their exceptional electronic and optical properties. Recent advances in the development of CMOS-compatible contacts for GaAs have paved the way for its integration with silicon-based technologies [1]. Metals such as nickel, platinum, and palladium are being extensively studied for their ability to form ohmic contacts through reactions with GaAs while satisfying the CMOS processing requirements [2]. Among these materials, nickel-based compounds have emerged as a particularly attractive contact material due to their excellent adhesion, low contact resistance, and ability to form uniform metallizations [2]. The use of new materials for nanoscale applications requires precise control of interfacial phenomena such as diffusion, reaction, and phase formation. As device dimensions decrease, it becomes imperative to understand and control the physical properties and stability of interfaces at the nanometer scale.

A thorough investigation of metal–semiconductor contacts is therefore essential for advancing the design and fabrication of scaled devices based on III-V compound semiconductors. The solid-state reaction between nickel thin films and GaAs substrates has been extensively studied. The first phase to form is the hexagonal $Ni_3GaAs$ phase [3]. The growth of the $Ni_3GaAs$ phase is diffusion-controlled and nickel is the predominant diffusing species whereas gallium and arsenic remain essentially immobile [3]. However, the mechanism of atomic diffusion in this phase still remains to be clarified.

In this study, the growth mechanisms of the $Ni_3GaAs$ phase are studied for two samples with Ni films of 20 nm and 100 nm of Ni deposited on GaAs. The initial stages of growth and the kinetics of the $Ni_3GaAs$ phase have been studied using in situ X-ray diffraction (XRD) measurements, transmission electron microscopy (TEM), and atom probe tomography (APT) analysis (Fig. 1a). Two interface configurations were examined: one with a coherent Ni/GaAs interface and the other with an incoherent interface. We validate the hypothesis that variations in XRD integrated intensity are proportional to the thickness of the formed phase by performing direct measurements using TEM and in situ XRD (Fig. 1b). In situ XRD measurements were then carried out during isothermal annealing at different temperatures on two samples with Ni film thicknesses of 20 nm and 100 nm, in order to monitor the growth kinetics of the sole $Ni_3GaAs$ phase formed.

By comparing these findings with nucleation and growth models, we conclude that the growth of the $Ni_3GaAs$ phase at the Ni/GaAs interface is predominantly diffusion-controlled at low temperatures and larger thicknesses (Fig. 1c), whereas it is mainly governed by interface reactions at higher temperatures and smaller thicknesses. The results indicate that the Ni vacancy diffusion mechanism is dominant in this phase, and that there is strong agreement between the $Ni_3GaAs$ growth kinetics observed in nano thin films and those reported for bulk diffusion couples. A possible diffusion mechanism is proposed.

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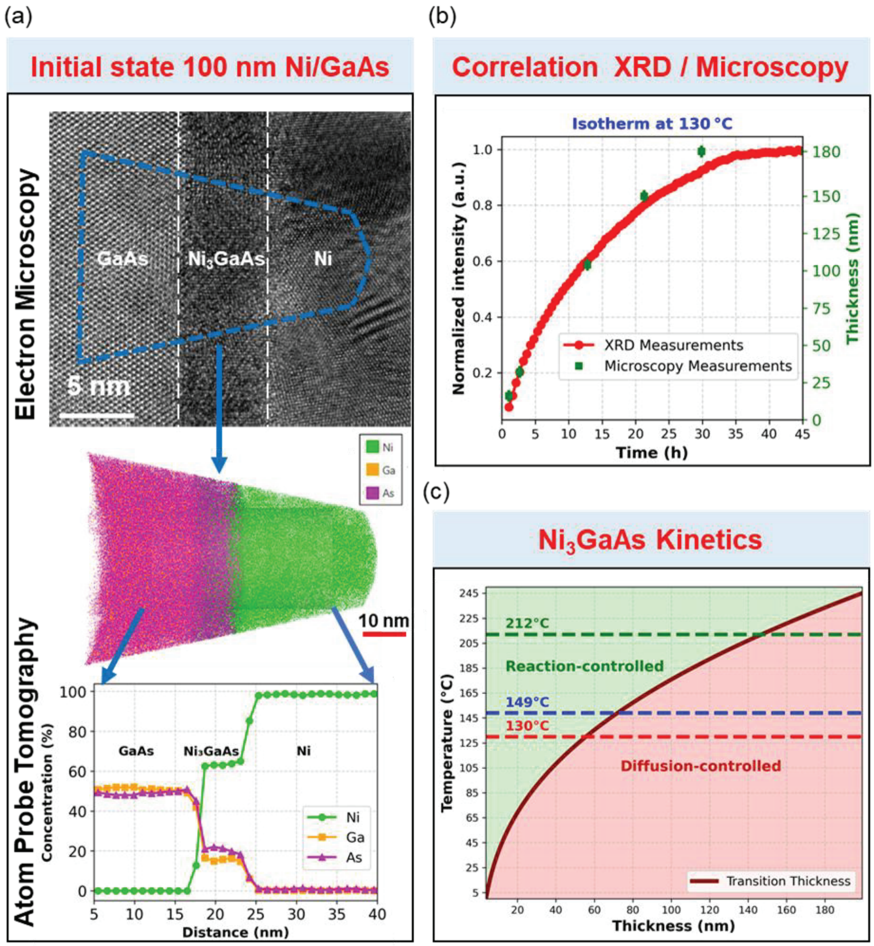

Fig. 1. (a) HRTEM and APT characterization of the samples in their as-deposited state for 100 nm Ni/GaAs sample showing a crystalline interfacial layer (b) Variation of the normalized integrated intensity (red curve with circle)) of the $Ni_3GaAs$ XRD peak as a function of time during isothermal annealing at 130°C, along with the thickness variation measured directly by TEM (green squares) using an in-situ XRD measurement stopped after different annealing times at 130°C. (c) Variation of the "transition temperature" between linear and parabolic regime with thickness. The variation of the thickness of $Ni_3GaAs$ formed during isothermal (130,149 and 212°C) is represented with dash lines.

# Development of the Aluminium Hybrid Bonding

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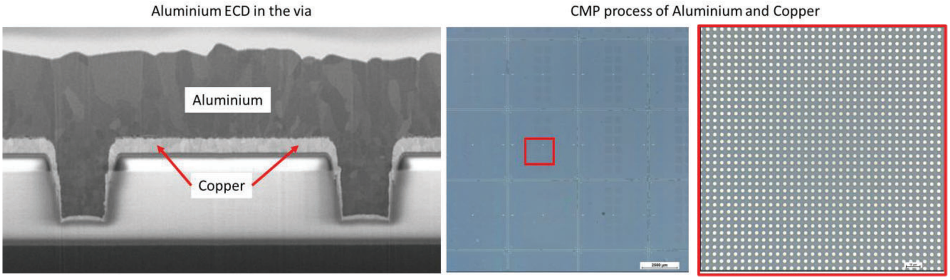
Aluminium-to-aluminium (Al–Al) direct bonding offers a CMOS compatible alternative to gold (Au–Au) and copper (Cu–Cu) bonding, avoiding metal cross-contamination in semiconductor process lines. While Au and Cu bonding benefit from negligible or controllable oxide formation, aluminium rapidly forms a native oxide upon air exposure, posing significant challenges for low-temperature bonding. Overcoming this limitation would enable heterogeneous integration of diverse sensors directly onto CMOS wafers.

Efforts have been made towards homogeneous and low temperature bonding with Al-Al surfaces. For instance, an EVG® 580 ComBond® tool (developed by EV Group), which enables low temperature (~ 100 °C to 150 °C) bonding under a high vacuum between two metal surfaces [1]. However, it has not yet demonstrated a hybrid bonding approach with this tool using a combination of dielectric and metal materials. Another bonding approach utilised a thin passivation layer made of titanium (Ti) and Palladium (Pd) [2]. Metals enable good adhesion to Al and have been used as bonding interfaces to overcome oxide formation at the Al interface [3-4]. The next approach, native oxide layer passivation using the plasma process, has been investigated to delay the oxide formation on the Al surface and thus establish the Al-Al bond [5].

In this work, we present key processes for aluminium hybrid bonding, including aluminium electroplating in variable via sizes, surface oxide removal and passivation, along with preliminary studies of Chemical Mechanical Planarization of Aluminium vias (see Figure 1). The studies will allow metallic bonding to be achieved at temperatures below 300 °C under ambient conditions, demonstrating the feasibility of aluminium hybrid bonding for CMOS-compatible sensor integration.



Aluminium ECD in the via

CMP process of Aluminium and Copper

**Figure 1 Aluminium electrochemical deposition (left) and Aluminium and Copper Chemical Mechanical Planarization**

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# PFAS-free Polyimide Passivation Thin Films in Advanced Metallization Stacks: Advanced Characterization, FEM Modeling, and Comparison with Conventional Polymers

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Modern back-end-of-line (BEoL) metallization stack architectures incorporating environment-sensitive materials like porous low-κ dielectrics require robust top passivation layers to ensure their mechanical and chemical stability, thus enabling a good overall system reliability. While polymer thin films are conventionally deployed for such top passivation films, regulatory restrictions on PFAS-containing materials necessitate the adoption of novel, PFAS-free alternatives. Promising candidates which are already being introduced by industry, are PFAS-free polyimides. Those polyimides exhibit distinct thermo-mechanical behaviours, such as temperature- and strain-rate-sensitive elasticity (viscoelasticity) as well as temperature-dependent coefficients of thermal expansion (CTE). Additionally, their glass transition temperatures ($T_g$) deviate significantly from standard PFAS-containing polymers. In summary, the complex thermomechanical behaviour of those new PFAS-free passivation polymers differs substantially from their PFAS-containing predecessors and, of course even more so from the other inorganic BEoL metallization stack components. Because of this complex behaviour, the thermomechanical behaviour and interaction of these passivation thin films need to be studied using complex FEM models. The materials behaviour needs to be modelled in all necessary detail using complex material models. The latter ones need experimental input to be adequately parametrized.

This study introduces an advanced characterization and modelling workflow for PFAS-free polyimide passivation layers on industrial BEoL samples, featuring:

- temperature-dependent (-60°C and 250°C) dynamic nanoindentation experiments (nanoDMA, see e.g. [1]) for the viscoelastic characterization of the industrial polymer thin films
- *in-situ* SEM CTE measurements as a function of temperature to directly correlate thermal expansion with microstructural evolution (Fig. 1)
- modelling of Prony series-based master curves and shift-functions for the parameter extraction from experimental data to advanced FEM material models, [2].

Using these techniques, we compare the key properties (viscoelastic properties, CTE, and $T_g$) of PFAS-free polyimides in the temperature range between -60°C and 250°C against conventional PFAS-containing counterparts, currently used in production, revealing changes in thermal stability and mechanical material properties. The derived parameters are implemented into a multi-physics finite element (FEM) framework to simulate thermo-mechanical interactions of these polymer films within the BEoL metallization stack, enabling reliability predictions under operational conditions. As a first short summary, PFAS-free formulations show CTEs roughly 25% below legacy materials (Fig 2).

This work establishes the foundation for next-generation BEoL stack and passivation design, as these PFAS-free polymers will become integral parts of future BEoL architectures and to that, of course, interact directly with the complex thermo-mechanical behaviour of the full stack.

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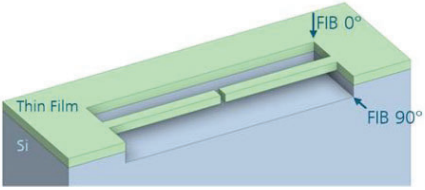

Figure 1: Sample schematic of the *in-situ* SEM CTE Design of Experiment.

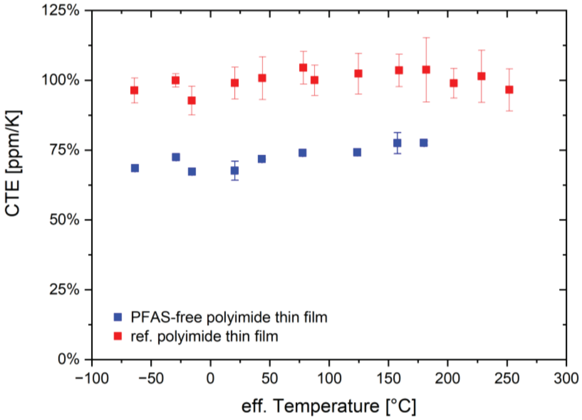

Figure 2: Comparison the temperature-dependent CTEs of PFAS-free and traditional polyimide passivation thin film characteristics.

# Pole figure measurements in grazing-incidence configuration for characterizing thin film texture

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## Synopsis

Grazing incidence wide-angle X-ray scattering is presented as an innovative approach to measure X-ray diffraction pole figures, enhancing sensitivity to nanoparticle and thin film texture compared to conventional Schulz geometry. Tuning the grazing incidence angle is utilized to obtain texture information at different depths in thin films.

## Introduction

X-ray diffraction pole figure measurements are essential to analyse crystallographic texture in thin films and nanoparticles, with applications in a wide array of material science fields. In lab- and synchrotron-based setups, pole figures are conventionally measured using equal incident and exit angles (θ-2θ or Shulz geometry) well-beyond the critical angle of the studied material. This geometry features a large X-ray penetration depth, decreasing the pole figure sensitivity to thin films or supported nanoparticles. In addition, the necessity to tilt the sample stage out of the horizontal plane during pole figure measurements in Schulz geometry makes *in-situ* experiments rather challenging.

This study demonstrates the use of grazing-incidence wide-angle X-ray scattering (GIWAXS) to acquire pole figures that are more sensitive to the near-surface region compared to pole figures measured in classic Schulz geometry. Pt thin films and nanoparticles on a MgO single-crystal substrate are used to showcase this method.

## Results

GIWAXS patterns are recorded continuously while rotating the sample azimuthally in its own plane (Fig. 1a). The near-horizontal sample orientation during GIWAXS – only tilted by the small incident angle – enables a more facile implementation of reactor chambers for in situ metrology compared to conventional Schulz geometry. Each measured 2D GIWAXS pattern contributes a line to the pole figure (Fig. 1b-c), and pole figures at different q-values (or equivalently 2θ-values) can be measured simultaneously. Figure 2 demonstrates the increased sensitivity to supported Pt nanoparticles with respect to the MgO substrate when using a grazing-incidence beam. It is seen that by decreasing the incident angle α below the MgO critical angle for total external X-ray reflection, the intensity of the Pt (111) diffraction spot is raised above the intensity of the MgO (111) diffraction spot, increasing the sensitivity to the targeted Pt signal while limiting the MgO background signal.

This increased sensitivity to the surface region is caused by the decreased X-ray penetration depth at small incident angles (Fig. 3a). This principle can also be utilized to study the crystalline texture at different depths inside a thin film. As an example, Figure 3b shows Pt 111 pole figures for a 50 nm (001)-oriented epitaxial Pt film on a MgO support recorded at an incident angle below and above the Pt critical angle. Below the critical angle, only the top few nanometers are probed, consisting exclusively of (001)-oriented grains. Above the Pt critical angle, the deeper X-ray penetration unveils extra diffraction spots, caused by (122)-oriented Pt grains presumably situated at the film-substrate interface.

## Conclusion

The increased sensitivity to the near-surface region of a grazing-incidence X-ray beam, combined with the simpler measurement geometry and the capability of depth profiling, prove grazing-incidence pole figures to be powerful for future *in situ* and *ex situ* texture analysis on thin films and supported nanoparticles.

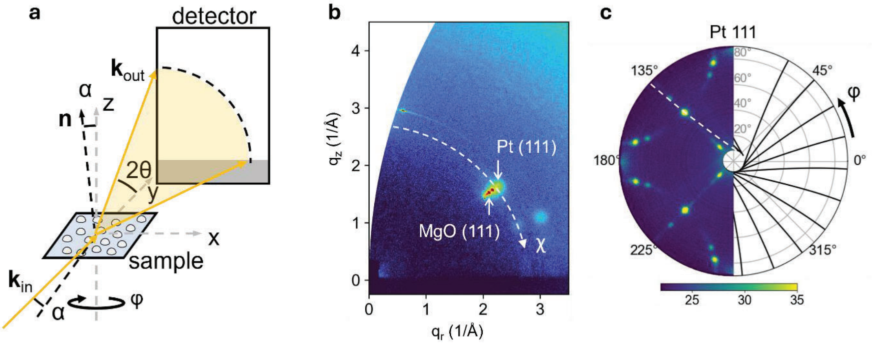

Figure 1: Grazing-incidence geometry and pole figure reconstruction. **a**: Detection of the X-ray diffraction cone. **b**: GIWAXS pattern for supported Pt nanoparticles. The white dashed line marks the contribution to the Pt 111 pole figure. **c**: Constructing a pole figure by scanning while rotating the sample. The black lines mark the contributions of individual scans.

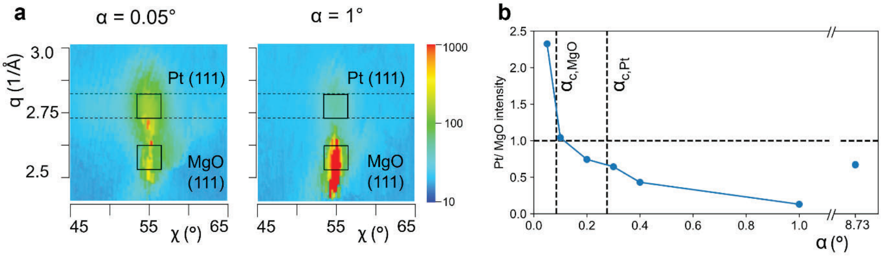

Figure 2: Pole figure sensitivity towards Pt nanoparticles compared to the MgO support. **a**: Reciprocal space cuts through the Pt and MgO (111) diffraction spots recorded at two incident angles (α=0.05° and α=1°). **b**: Ratio between the Pt and MgO (111) diffracted intensity versus incident angle, showing that the intensity of the Pt (111) diffraction spot is raised above the intensity of the MgO (111) diffraction spot when going below the critical angle of MgO ($\alpha_{c,MgO}$). The point at α=8.73° is measured in Schulz geometry.

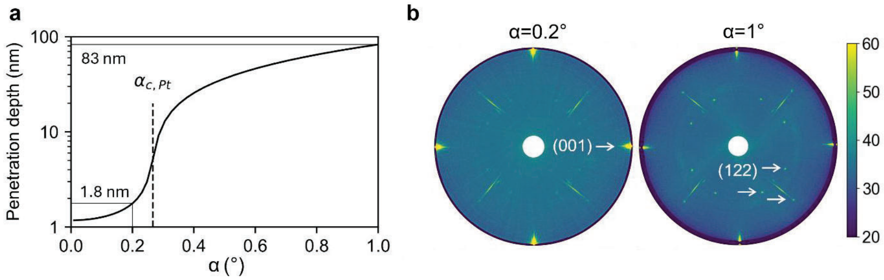

Figure 3: Selecting the information depth. **a**: X-ray penetration depth in Pt versus the incident angle. **b**: Pt 111 pole figures for a 50 nm (001)-oriented epitaxial Pt film recorded at two incident angles. At α=0.2° (i.e. below $\alpha_{c,Pt}$), the limited X-ray penetration depth in the film generates sensitivity to Pt crystals situated in the near-surface region only, leading to diffraction spots of (001)-oriented Pt. Well-beyond $\alpha_{c,Pt}$, X-rays penetrate through the entire Pt film, generating sensitivity for crystals at the near-surface, bulk and Pt-MgO interface. At α=1°, specifically, additional (122)-oriented Pt diffraction spots become visible, which can be linked to textural components at the interface region.

# Investigating local stoichiometry fluctuations in nm-thin semiconductor alloys: a case study on SiGe

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Semiconductor alloys allow tuning the electronic properties by changing the alloy composition. This adjustability makes them attractive materials for a wide range of applications. Thin layers of SiGe are of interest in semiconductor devices such as heterojunction bipolar transistors and field-effect transistors. When one or more dimensions are reduced to the nanoscale, local composition fluctuations in such alloys become crucial.

Using first-principles density functional theory[1] and the computationally faster extended Hückel theory[2], we simulate a large number of atomic structures to quantify the effect of local stoichiometry fluctuations on the band structure. We study unstrained alloys as well as alloys biaxially strained along the ⟨100⟩ directions. Our results show how introducing small fractions of carbon, which reduce the lattice mismatch with the Si substrate, lowers the band gap of the alloy. When carbon atoms occupy adjoining lattice sites, defect states are observed, which significantly reduce the band gap. However, by calculating the formation energy, we conclude that such atomic structures are energetically unfavorable.

By simulating few-nm thin SiGe layers sandwiched between Si, we show how the concept of an effective layer thickness can be used to describe the quantum confinement effect. Quantum confinement increases the band gap with decreasing layer thickness, counteracting the band gap reduction from increasing the Ge content. Applying results from the bulk alloy, we show how the numerical model of the finite quantum well can be used to describe the effect of local stoichiometry fluctuations on the band gap of thin layers. This model is in good agreement with results from calculations of multiple atomic structures of various alloy compositions and layer thicknesses.

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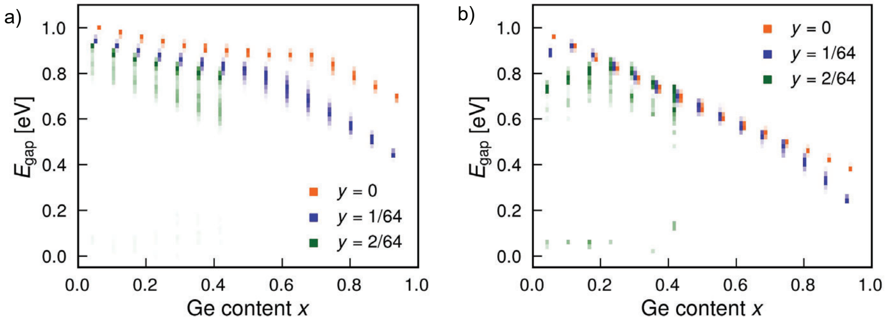

Figure 1: Band gap of unstrained (a) and ⟨100⟩ biaxially strained (b) $Si_{1-x-y}Ge_xC_y$ alloys as a function of the alloy composition. The shaded region depicts the variation in band gap observed from the simulation of 200 atomic structures.

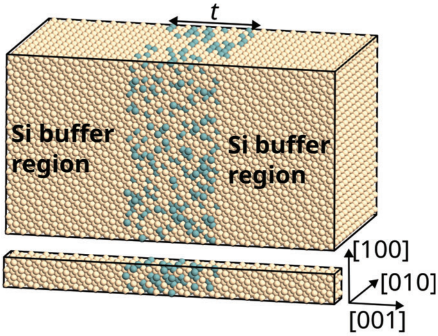

Figure 2: Example of the simulated atomic structure of a 3 nm thin SiGe layer between Si. Beige atoms are Si, green atoms are Ge.

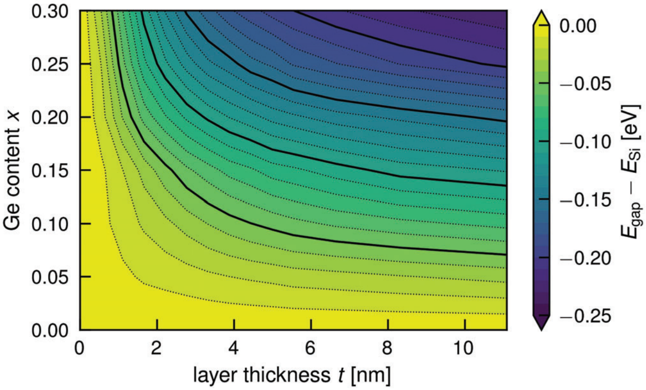

Figure 3: Effect of alloy composition and layer thickness on the band gap of biaxially strained SiGe layers. It is calculated as the mean value of 36 atomic structures.

# Pt redistribution in Ni(Pt)Si layers obtained via total vs partial reactions and its impact on specific contact resistivity

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Ni(Pt)Si layers are often used as contact layers in CMOS technologies. Historically, they were obtained using a single annealing. Currently, the associated process is rather based on two annealings, allowing to perform partial reactions, meaning that not all the deposited metal is of actual use [1]. After metal deposition, the first annealing is performed, during which part of the deposited Ni layer reacts with the substrate. It is followed by a selective etch, which removes the remaining metal. The second annealing allows to obtain the desired low-resistive Ni(Pt)Si phase. The impact of this change in terms of grown Ni(Pt)Si layer properties and associated contact performances is not well known. Yet, the redistribution of Pt in the system should be impacted, since Pt is expected to segregate at the $Ni_{1-x}(Pt)Si_x$ surface, a mechanism known as the snowplow effect [2].

In order to gain understanding on this topic, $Ni_{0.9}Pt_{0.1}$ metal layers of various thicknesses were deposited on top of 300 mm n-doped Si(100) wafers. A two-step annealing process based on rapid thermal annealings (RTA) was defined: RTA1 at 230 °C for 20 s and RTA2 at 390 °C for 30 s. The first annealing should consume around 5 nm of $Ni_{0.9}Pt_{0.1}$. The thickness of the deposited metal layer was varied from 5 nm to 22 nm (see Fig. 1), allowing not only to compare a total vs a partial reaction, but also to understand the role of the available metal reservoir. The layers were characterized after RTA1 and RTA2 via XRD measurements. After RTA2, additional XRR, SEM and TOF-SIMS measurements were performed. The same set of conditions was then applied on patterned wafers defining TLM structures [3]. The specific contact resistivity ($\rho_c$) of the n-doped Si/$Ni_{1-x}(Pt)Si_x$ interface was obtained and complementary TEM analyses were performed on two relevant samples.

On blanket wafers, it is shown that the thickness of the Ni(Pt)Si layers obtained using the procedure described here above is equivalent for all the samples, despite slightly lower for S1 and, in a lesser extent, S2 (see Fig. 1). The layers present a similar texture, with two preferential orientations out of the plane along the [010] and [013] crystalline directions, and some degree of epitaxy (not shown). Such a texture is indicative of a growing mechanism involving the sequential development of nanocrystalline phases (see also XRD data collected post RTA1, presented Fig. 2). However, the average diameter of the grains composing the Ni(Pt)Si layers and obtained via SEM image analysis (not shown) varies along the samples. The biggest grains are obtained for sample S1, with a mean value of 77 nm ± 33 nm, for then quickly drop (mean value of 45 nm ± 18 nm for S2 and 42 nm ± 13 nm for S5). More importantly, the redistribution of Pt is not equivalent for all samples. As expected, Pt strongly segregates at the Ni(Pt)Si surface (see Fig. 3(a)ii)). But, overall, less Pt is incorporated in S1 and, in a lesser extent, S2. Additionally, S1 is the only sample showing a slight Pt signal at the bottom Ni(Pt)Si/Si interface (see Fig. 3(b)). On patterned wafers, it is shown Fig. 4(a) that $\rho_c$ is not equivalent for all the samples, with best results obtained for partial reactions. While some trends are not preserved as compared to blanket wafers (sample average grain size, see diffraction patterns presented Fig. 4(b)), Pt atom redistribution is clearly impacted (see Fig. 4(b), EDX maps). The presence of Pt atoms at the bottom Ni(Pt)Si/Si interface is proposed to drive $\rho_c$ observed differences.

**Acknowledgements:** Part of this work, carried out on the Platform for Nanocharacterisation (PFNC), was supported by the ‘‘Recherche Technologique de Base’’ and ‘‘France 2030 - ANR-22-PEEL-0014’’ programs of the French National Research Agency (ANR).

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|  | Sample name |  |  |  |  |
|---|---|---|---|---|---|
|  | S1 | S2 | S3 | S4 | S5 |
| Deposited metal thickness (nm) | 5 | 7 | 10 | 14 | 22 |
| **XRR results** |  |  |  |  |  |
| Ni(Pt)Si layer thickness (nm) | 11.4 | 11.8 | 11.9 | 11.9 | 11.9 |
| Ni(Pt)Si layer roughness (nm) | 3.8 | 3.5 | 2.8 | 2.5 | 2.4 |
| Ni(Pt)Si layer density (g/cm³) | 20.1 | 20.7 | 20.8 | 20.6 | 21.0 |
| Top layer | 7.1 | 7.5 | 7.7 | 7.8 | 7.9 |
| Middle layer | 6.5 | 6.7 | 6.7 | 6.6 | 6.7 |
| Bottom layer | 6.5 | 6.4 | 6.3 | 6.2 | 6.4 |

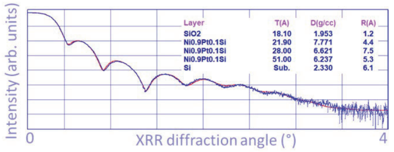

Fig. 1: Presentation of the studied samples and corresponding XRR results post RTA2 (top). Example of data fitting for S3 (bottom). The fits are performed using a 3 layers model, which should reflect the expected Pt gradient within the Ni(Pt)Si layer. The given layer thickness values are the sum of the 3 contributions. Due to air break between RTA2 and XRR measurement, a $SiO_2$ layer is added on top of the structure, in order to account for oxidation phenomena. The given layer roughness values are the sum of all contributions.

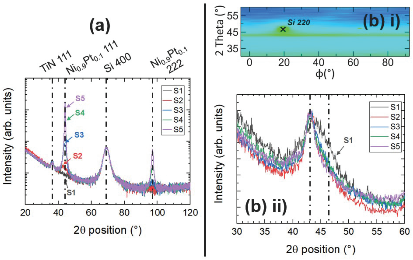

Fig. 2: XRD results obtained post RTA1, before selective etch. (a) Out-of-plane acquisition in ω-2θ configuration. (b) i) In-plane reciprocal space map (IPRSM) of sample S4, given here as an example. All the samples show the same signature, i.e. a weak signal arranged along a fiber texture around 43°. ii) IPRSM diffraction signal integrated over the whole investigated φ range for the whole sample set, with the Si epitaxial spots cut out in the process in order to avoid their parasitic contribution. No strong signal that would be associated to a grown Ni-rich phase is seen, neither in-plane nor out-of-plane, which means that the layer presents a nano-crystalline structure.

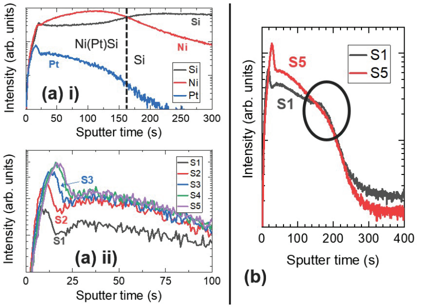

Fig. 3: (a) TOF-SIMS analysis using a primary $Bi_3^+$ ion source and $Cs^+$ sputtering source showing i) a general overview of the system (example of S4) and ii) a comparative study of Pt segregation amount at the top interface. The bottom Ni(Pt)Si/Si interface is not resolved with this acquisition conditions. (b) Comparative Pt TOF-SIMS analysis using a primary Cs- ion source of S1 and S5. The bottom interface is resolved and shows the presence of Pt atoms for S1 only.

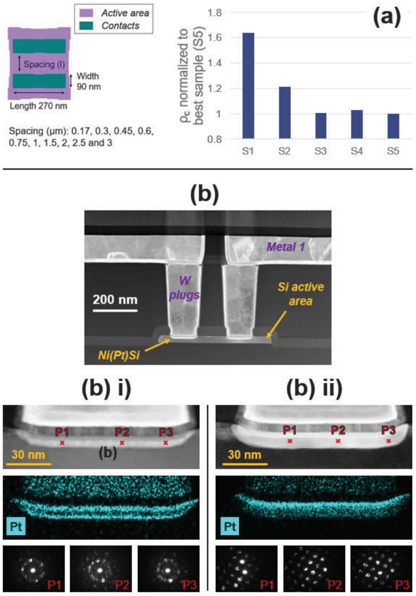

Fig. 4: (a) Top-view of the TLM design used for electrical characterization (left). Degradation of the specific contact resistivity when available metal for siliciuration is reduced, with $\rho_c$ = 4.9E-8 Ω.cm² for S5 (right). (b) BF-STEM image of a representative TLM motif and zoom on the contact area with associated Pt EDX mapping and diffraction spots for contact process conditions equivalent to i) sample S1 (total reaction) and ii) sample S4 (partial reaction).

# Assessment of defects and quality of thin films and interfaces with laser-based thermoreflectance thermal conductivity measurements

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Mitigating temperature rises in 3D integrated circuits (IC) has resulted in thermal challenges across a wide range of manufacturing length scales, from the middle- to back end-of-line in the metals and dielectrics used for interconnects, hybrid bonds, and heat spreaders. This problem is compounded by the fact that the reduced dimension of materials compounded with defects and non-idealities that arise from heterogeneous integration and interfaces all lead to increased thermal resistances, and thus increased temperature rises. Thus, minimizing 3D IC temperature rises is directly correlated to ensuring that materials and interfaces that are fabricated across all length scales in a 3D IC have increased thermal conductivities and decreased interfacial thermal resistances (ITR), which is directly correlated to the density of defects and voids in the thin films and interfaces.

The first problem to mitigate thermal resistances of 3D ICs is to minimize reductions in thermal conductivity of low dimensional metals. Both the thermochemical and thermomechanical stability of Cu at these length scales, along with the strong reduction in both electrical and thermal conductivity due to length scales reducing to those less than its electronic mean free path has led to underperformance, which in part can be ascribed to deleterious heating effects.[1] While Ru and W interconnects are currently being evaluated, a range of additional metals and metallic systems (alloys, eutectics, 2D materials, and multilayers) are also of note due to their potential mechanical and thermal properties that are superior to Cu at the < 100 nm length scale. In this presentation, we will discuss our recent efforts in measurements of thermal conductivity and electron-phonon scattering rates of thin metal films for interest as next-generation metal interconnects,[2] including Ru, W, Ir, Pt, Mo, Co and Ta, along with 2D delafossite films and metal multilayers. We will discuss the use of various thermoreflectance techniques – including time-domain thermoreflectance (TDTR), frequency-domain thermoreflectance (FDTR), steady state thermoreflectance (SSTR),[3,4,5] and *Laser Thermal's* FASTR tool – to measure the thermal properties of thin films, including the in-plane a cross plane thermal conductivity of thin films of metals, dielectrics, multilayer metals, and 2D systems. We will show that the thermal conductivity measurements are directly related to defects and microstructure of these thin films, offering a unique, high-throughput assessment of film quality to aid in selection of metal interconnects.

The second problem to mitigate thermal resistances of 3D ICs is fabricating electrically insulating films (e.g., amorphous dielectrics, and AlN), from nanometer to micrometer scales, in contact with silicon while maintaining a combination of high thermal conductivity (for heat spreading) or low ITR (for hybrid bonding). This problem applies to a range of length scales and materials, ranging from the ITRs between amorphous dielectrics and/or metals used in hybrid bonds, to achieving high thermal conductivity electrical insulators in contact with Si for heat spreaders (e.g., AlN). With our thermoreflectance-based approaches, we will demonstrate the ability assess film and interface quality, including high thermal conductivity AlN films,[6,7] and dielectric and metal films buried hybrid bonded interfaces,[8] using measurements of thermal conductivity and ITR of nanoscale films both at the surface and interfaces that are buried sub-surface.

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# Low-Pressure HF Vapor MACE of Silicon Nanowires: Pt vs Pd Catalyst Effects on Morphology and Etch Rate

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Metal-assisted chemical etching (MACE) has emerged as a versatile route for fabricating low-dimensional, porous silicon nanostructures for photonics, optoelectronics, and sensing. It offers comparatively simple and cost-effective processing relative to anodic or stain etching but still relying predominantly on liquid-phase chemistries [1]. Previous studies have demonstrated that Pd-assisted chemical etching in aqueous HF/$H_2O_2$ can form well-aligned porous silicon nanowire arrays even on lightly doped p-type substrates, thereby overcoming doping constraints typical of Ag- and Au-based systems [2]. However, liquid-phase Pd-MACE still suffers from challenges such as mass-transport limitations, capillary-induced collapse, and limited control over pore morphology, which hinder scalability and precise shape engineering of nanowires.

In this work, a Pd-assisted MACE process in HF vapor phase is proposed for the first time, with the aim of achieving controlled growth of silicon nanowires (SiNWs) and enabling direct comparison with established vapor-phase Pt-MACE routes. Building on prior vapor-phase demonstrations where HF/$H_2O$ vapor and ambient oxidizers drive localized, metal-catalyzed gas–solid etching to produce high-aspect-ratio nanowires [3], the present study replaces Pt with Pd as the catalyst to explore differences in etch rate, porosity, and nanowire morphology under otherwise comparable process conditions. Initial experiments use Pt-MACE-derived SiNWs as a reference and then systematically investigate Pd-MACE behavior in HF vapor, focusing on how the catalyst type, HF activity, and moisture content influence porosity formation as well as nanowire straightness and verticality.

The proposed study aims to map the process window in which Pd-MACE in vapor phase can generate vertically aligned, porous SiNWs with tunable diameter and porosity, while mitigating structural collapse and improving pattern transfer fidelity. By directly comparing Pt- and Pd-catalyzed HF vapor etching on similar defined patterns, the work seeks to reveal catalyst-dependent etching characteristics and identify regimes in which Pd offers advantages for porous Si nanowire engineering. The anticipated outcome is a novel, vapor-phase Pd-MACE platform that combines the materials flexibility of Pd-cataylst wet MACE with the morphology-control and stiction-free advantages of gas-phase processing, opening pathways to scalable nanowire-based photonic, sensing, and energy devices.

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# Low-temperature formation of ultra-thin Co disilicide ($CoSi_2$) layers for advanced CMOS applications

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The transition from 4G to 5G in the coming years will enable new forms of the Internet of Things, notably the broader deployment of autonomous vehicles. This therefore requires the development of new microelectronic circuits based on MOS-type transistors (Metal Oxide Semiconductor) with gate widths of 65 nm and below. Silicides are intermetallic layers formed during annealing by reactive diffusion between a metal (Ni, Co, Ti, W, etc.) and silicon in order to be used at transistors contacts [1]. The formation of silicides helps to reduce the contacts resistance of the transistor gate, which is inversely proportional to the maximum frequency of the devices. However, for advanced CMOS technologies (gate width < 65 nm), problems arise in the formation of $CoSi_2$ (the least resistive phase) at the transistor gate. Indeed, the formation of $CoSi_2$ is preceded by the formation of the intermediate CoSi phase by reactive diffusion at a lower temperature. The $CoSi_2$ phase growth is controlled by nucleation at the triple junctions of the CoSi phase. Consequently, the downscaling of gate dimensions reduces the number of nucleation sites to form $CoSi_2$, hence narrow line effect occurs (Fig. 1) [2]. Moreover, when the gate dimension is reduced, the junction depth is also minimized to control the junction silicon consumption. The maximum of silicide thickness downs to 20 nm, inducing severe degradation of thermal stability i.e. agglomeration phenomena at a certain temperature [3].

In the present paper, the silicide layers are formed though the SALICIDE (SelfAligned saLICIDE) process (Fig. 2). It can be summarized in five principal steps: Surface preparation, Co – TiN metal deposition, RTA1 (rapid thermal annealing 1), selective etch of non-reacted metal and RTA2 step to form $CoSi_2$. For 7 nm Co, 23 nm $CoSi_2$ is expected after a total reaction of the metal. Since the thickness of $CoSi_2$ is directly proportional to the thickness of CoSi, it is possible to obtain a thinner $CoSi_2$ layer by reducing the RTA1 temperature to form less CoSi. This is called partial silicidation or partial reaction. As we wanted to reduce the $CoSi_2$ thickness, RTA1 temperature was reduced in the range of 400 °C to 500 °C. The RTA2 temperature used is 790 °C. As shown in Fig. 3, for RTA1 temperature up to 460 °C, partial reaction occurs (Co is not fully consumed during silicidation). Beyond this temperature, the reaction is total (Co is fully consumed). At the same time, the sheet resistance increases for thinner layers (Fig. 4). The TEM/EDX images show the non-continuity of the thinner silicide layers: the layers are agglomerated (Fig. 5).

To assess the influence of RTA2 temperature, several RTA1 temperatures (RTA1 410 °C, 440 °C, and 500 °C) have been kept for further studies. For RTA1 at 410 °C, the $CoSi_2$ thickness remains constant at around 12 nm in the range of 585 °C and 790 °C of RTA2 temperature. The CoSi layer is fully transformed into $CoSi_2$ even at the lowest RTA2 temperature (585 °C). For RTA1 at 440 °C and 500 °C, the $CoSi_2$ thickness evolves with RTA2 temperature, indicating that CoSi continues to be transformed into $CoSi_2$ during the annealing treatments (Fig. 6). For all RTA1 temperatures, the sheet resistance is very high at low RTA2 temperatures and then stabilizes from an RTA2 temperature of about 615 °C (Fig. 7). In fact, TEM/EDX images reveal a bilayer structure of approximately 7 nm CoSi / 10 nm $CoSi_2$ for RTA1 440 °C and 500 °C (Fig. 8).

In the full paper, we will present TEM-EDX and HR-SEM observations to evaluate the formation and the thermal stability of ultra-thin $CoSi_2$ layers in the frame of advanced CMOS technologies.

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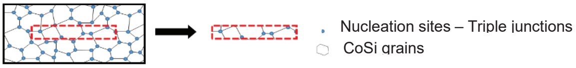

*Fig. 1: CoSi grains and $CoSi_2$ nucleation sites (triples junctions)*

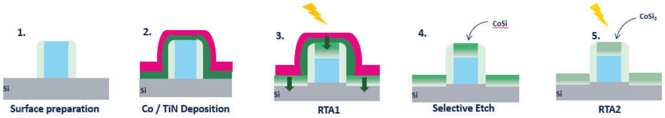

*Fig. 2: $CoSi_2$ SALICIDE process*

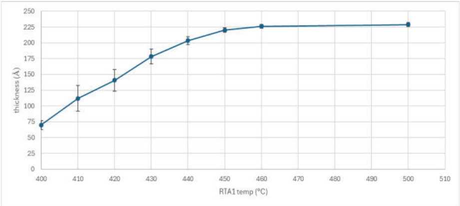

*Fig. 3: $CoSi_2$ Thickness vs RTA1 temperature*

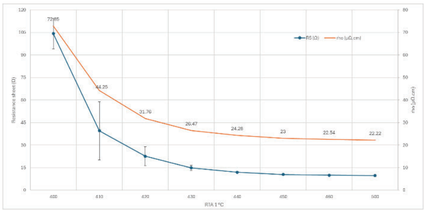

*Fig. 4: Sheet resistance Rs and resistivity rho vs RTA1 temperature*

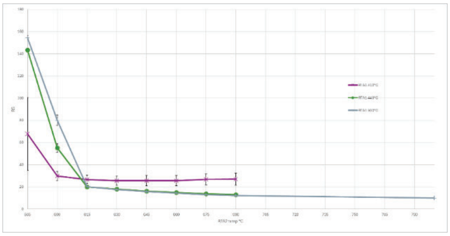

*Fig 5: TEM image of agglomerated $CoSi_2$ layer corresponding to RTA1 400 °C*

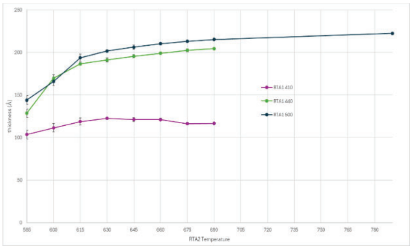

*Fig. 6: $CoSi_2$ Thickness vs RTA2 temperature for RTA1 400 °C, 440 °C and 500 °C*

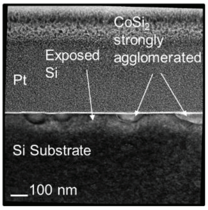

*Fig. 7: $CoSi_2$ sheet resistance Rs vs RTA2 temperature for RTA1 400 °C, 440 °C and*

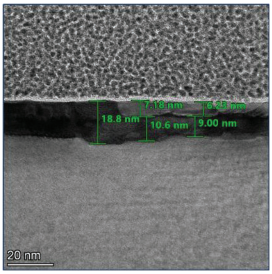

*Fig 8: TEM image of* ~ 7 nm CoSi / 10 nm $CoSi_2$ for RTA1 at 440 °C *and*

# Magnetic Tunnel Junctions Based on Chiral Self-Assembled Monolayers

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The chirality-induced spin polarization (CISS) effect has been described first by R. Naaman and D. Waldeck in 1999 [1]: tunneling of electrons through a chiral tunnel barrier results in a strongly spin-polarized electrical current. Since its discovery, the CISS effect has found many potential applications [2], e.g., in chromatography (enantiomer separation), energy conversion (water electrolysis), display technology (OLED) and spintronics. Basically, the physical effects of a chiral thin film on an electrical current correspond very much to that of a ferromagnetic or antiferromagnetic layer. Therefore, chiral thin films might serve as a simplified version of the rather complex stack used in state-of-the-art spintronics devices, such as STT or SOT MRAM [3] (Figure 1).

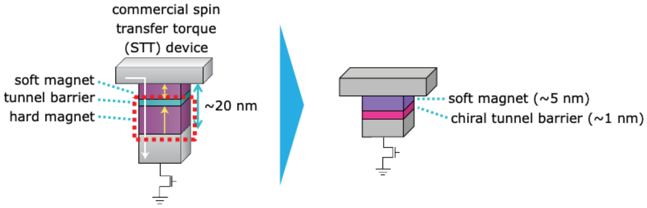


**Figure 1.** Design of a magnetic tunnel junction (MTJ) using a chiral self-assembled monolayer instead of a (anti)ferromagnetic pinned layer (PL) [3].

In principle, spintronic devices promise several advantages over other memory technologies: they are non-volatile, very fast switching (~1 ns), energy-efficient, and they have a small footprint on the chip (1T1MTJ) compared to, e.g., SRAM (6T). However, current commercial MRAM suffers from severe drawbacks such as a relatively low ON/OFF ratio (often <10) and a rather thick (up to 20 nm) pinned layer with a complex layer structure composed of materials which are difficult to process. This antiferromagnetic stack can be replaced by a much thinner (1 nm) chiral self-assembled monolayer (SAM).

The majority of functional SAMs described in the literature is based on thiols on gold substrates. This material combination is highly convenient to fabricate, but it has some serious drawbacks: thiol SAMs are quite sensitive to thermal and oxidative stress, and gold tends to diffuse in an uncontrollable manner. They are not even remotely suitable for a CMOS environment. Therefore, we are using 1,1'-binaphth-2-yl hydrogenphosphate (BNP) as a chiral building block, which is commercially available and readily forms robust covalent bonds to oxidic surfaces and is thus compatible to the most common materials used in semiconductor manufacturing processes (Figure 2). Phosphonate- and phosphate-anchored SAM are also robust enough for the deposition of a metallic top electrode, e.g., by sputtering [4].

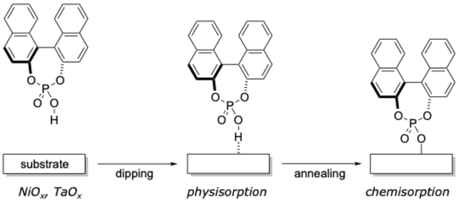


**Figure 2.** Covalent modification of oxidic substrates with *S*-BNP by a dipping process.

A first generation of chiral SAM-based MTJs using nickel substrates showed strong spin polarization (measured by cAFM or by eutectic gallium-indium alloy contacts) but needed a very high coercitive magnetic field (>0.5 T) to achieve the required out-of-plane magnetization. Therefore, we switched to Ta/CoFeB/MgO/Ta as a magnetic substrate. The BNP SAM was deposited onto the native $Ta_2O_5$ surface. For this device type a much lower coercitive field of 2-3 mT was sufficient to obtain complete out-of-plane magnetization. This device architecture is analogous to a commercial MRAM [5].

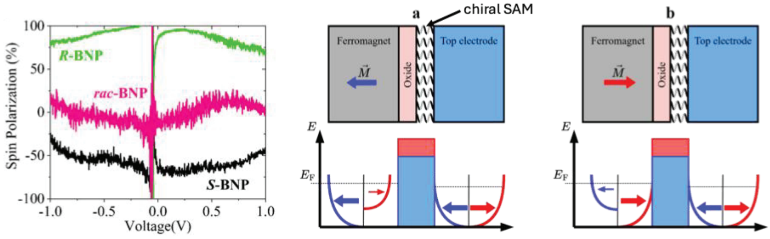
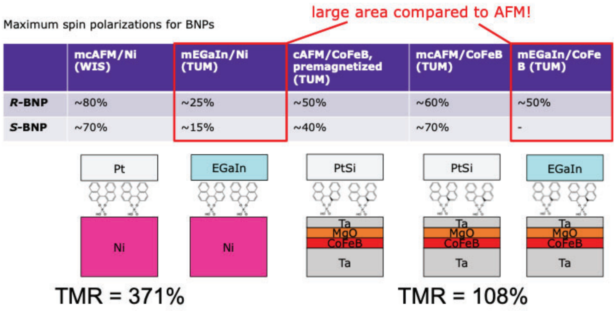


**Figure 3.** Voltage-dependent spin polarization of BNP on Ni (mcAFM) (*left*) and the tunneling model for MTJ adapted to the CISS effect (*right*).



large area compared to AFM!

Maximum spin polarizations for BNPs

| | mcAFM/Ni (WIS) | mEGaIn/Ni (TUM) | cAFM/CoFeB, premagnetized (TUM) | mcAFM/CoFeB (TUM) | mEGaIn/CoFeB (TUM) |
|---|---|---|---|---|---|
| ***R*-BNP** | ~80% | ~25% | ~50% | ~60% | ~50% |
| ***S*-BNP** | ~70% | ~15% | ~40% | ~70% | - |

**Table 1.** Overview of spin polarizations and TMR values of BNP on Ni and CoFeB/MgO substrates measured by various methods. The world record is a TMR of 631% [6], and for a typical commercial MRAM 180% have been reported [5].

In summary, we demonstrated that with a very thin (1 nm) and chemically robust chiral BNP SAM on Ni substrates magnetic tunnel junctions (MTJs) can be obtained. A preliminary study on CoFeB/MgO substrates - requiring a much lower coercitive field - indicates similar results. The spin polarization effect has been observed with various different types of top contact - conductive AFM (~20 x 20 nm$^2$) vs. EGaIn (~100 x 100 $\mu$m$^2$) contact - with contact areas differing by at least 6 orders of magnitude.

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# Study of Doping Methods and Ge-PAI Conditions on Ti Silicidation for Advanced FD-SOI Nodes

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In advanced technology nodes, the shrinking of the source/drain contact area leads to increasing concerns about the growing prominence of metal/semiconductor contact resistance [1]. To address this issue, pre-amorphization by implantation (PAI) performed prior to Ti metallization has been proposed as an effective technique in achieving low contact resistance [2]. However, the effect of the doping process together with the PAI on Ti-silicidation with high dopant concentration remains unclear, notably the extent to which the doping process affects the material structure and, in turn, the solid-state reactions.

In this work, we study the impact of doping process as well as different Ge pre-amorphization conditions on Ti-silicidation phase sequence. (100)Si substrates were P-doped using two different methods : A double P ion implantation (I/I) was carried out on a first half of the substrates ((i) 9 keV, $3x10^{15}$ at/cm² and (ii) 0.75 keV, $6x10^{14}$ at/cm²), while the other half was doped using a 30 nm in-situ n-doped (ISD) Si:P epitaxial layer with few $10^{21}$ atoms/cm$^3$. Dopants were then activated using spike annealing. In ISD layers, active P chemical concentration ($N_a$) of $7x10^{20}$ atoms/cm$^3$ was achieved. P-doped silicon substrates were pre-amorphized by Ge implantation at different conditions prior to Ti metallization. The evolution of the sheet resistance ($R_s$) as a function of (i) the rapid thermal annealing temperature and (ii) the thickness of the amorphous silicon (a-Si) is described in Figure 1.(a) in the I/I system and in Figure 1.(b) in the ISD system. Regarding the doping method combined with PAI conditions, results display different trend evolutions, notably within the 500 – 900 °C temperature range. For high-energy PAI samples, sheet resistance was dominated by the presence of a-Si at low annealing temperatures. Then, after an annealing at 600 °C, in the I/I doped system, all samples exhibited similar $R_s$ values, while in the ISD doped system, PAI-17 (as-deposited a-Si thickness was about 17 nm) and PAI-29 (as-deposited a-Si thickness was about 29 nm) samples exhibited lower $R_s$, compared to the reference (without PAI) and PAI-5 (as-deposited a-Si thickness was about 5 nm) samples. On the other hand, both systems were found to exhibit minimum $R_s$ values after an annealing at 800 °C, regarding the PAI-29 sample in the I/I doped system and the PAI-17 and PAI-29 samples in the ISD doped system. In order to correlate these electrical behaviors with solid state reaction, complementary in plane X-ray diffraction measurements (IP-XRD) were performed. Results are presented in Figure 2. The XRD pattern recorded after annealing at 600 °C, in the region where $R_s$ values were similar in the I/I-doped system, revealed diffraction peaks corresponding to the $Ti_5Si_4$ intermediate phase (identified with triangle symbols) whatever the initial a-Si thickness. In contrast, in the ISD doped system, diffraction peaks of C49-$TiSi_2$ (identified with square symbols) were observed in coexistence with the $Ti_5Si_4$ regarding the PAI-17 and PAI-29 samples, and this correlates with the decrease in $R_s$. In the two systems, the lowest $R_s$ value was assigned to the formation of the C54-$TiSi_2$ (identified with crescent moon symbols).

The a-Si created by Ge implantation is known to be partly consumed by Ti silicidation and partly recrystallized with solid phase epitaxial regrowth (SPER) [2]. According to the SPER kinetic, all the a-Si should be recrystallized after an annealing at 600 °C. Thus, regarding the discrepancies we highlighted, doping method may impact Ti silicidation phase sequence, in addition to the Ge PAI process. As widely studied in the 1990s [3], PAI was found to enhance silicidation at lower temperatures. However, phase sequence in samples doped using in-situ epitaxial method may not undergo the same phase formation kinetic as in the ion-implantation doped sample.

The impact of doping method together with PAI conditions was studied. PAI enhanced Ti-silicidation at lower temperatures in both systems. Interestingly, the doping method was found to impact Ti silicidation too. Results suggest that the phase formation kinetics in ISD samples may be faster than those in I/I doped samples with promoting phase coexistence.

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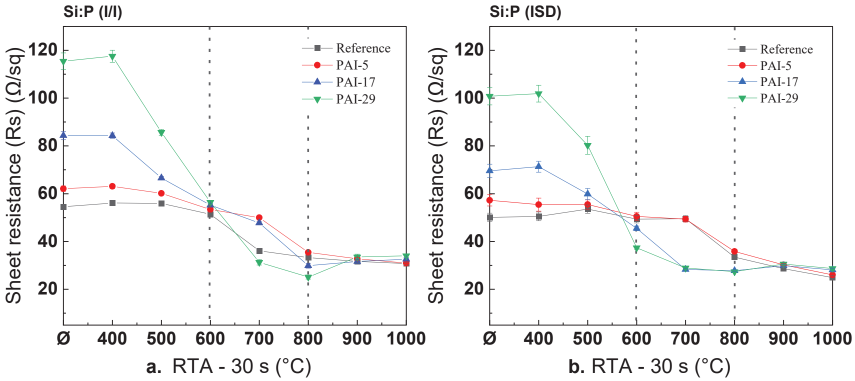

Figure 1. Evolution of the sheet resistance $R_s$ as a function of the annealing temperature for all investigated (a) ion-implantation doped samples and (b) in-situ doped samples. Samples were annealed for 30 s in $N_2$ atmosphere.

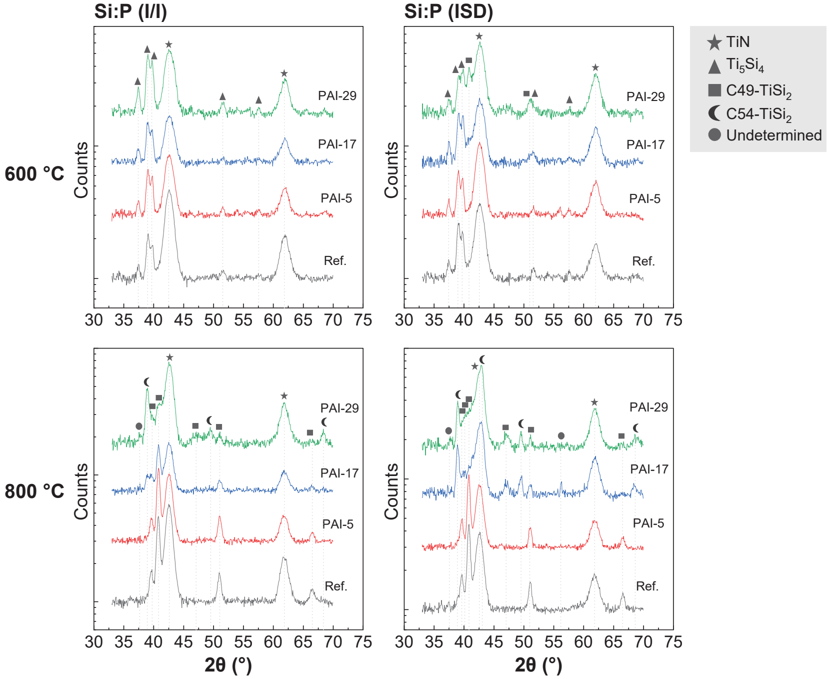

Figure 2. In-plane X-ray diffraction patterns for different Ge PAI conditions, after an annealing at 600 °C (top) and 800 °C (bottom) for the ion-implantation doped system (to the left) and the in-situ doped system (to the right). Samples were annealed for 30 s under $N_2$ atmosphere.

# Crystallization investigations of Ge-rich GST cells using *in situ* thermal pulses coupled with STEM-EDX and HR-TEM analyses

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Phase Change Materials composed of ternary alloys, commonly $Ge_2Sb_2Te_5$ (GST), are considered to replace classical non-volatile memories in various applications. The growing interest in this technology is related to the significant difference in physical properties between the amorphous and crystalline phases, which allows for easy modification and reading of the memory state, coupled with a fast-switching capacity of the order of ns. Typical crystallization temperature for GST is in the range of 150-170°C, a temperature too low for data retention in automotive applications. To address this limitation, Ge-rich GST (GGST) alloy with a crystallization temperature of 350°C was developed [1]. This material crystallizes incongruently, and ramp annealing at low heating rates [2] show the presence of crystallized Ge and GST.

In order to investigate the phase separation in conditions closer to the working conditions of memories (i.e. ns timescale), rapid heating experiments are performed by applying brief thermal pulses of 0.3s to GGST amorphous confined nanostructures, *in situ* in TEM/STEM microscopes. STEM-EDX analyses have been performed after each thermal pulse to follow the evolution of the spatial distribution of Ge, Sb and Te as a function of the temperature, within the cell. While the Sb concentration remains quite homogeneous regardless of temperature, inhomogeneities in Ge and Te compositions are evidenced from 320°C on (Fig. 1A and 1B). A local increase in Te content is observed in the periphery of the cell, close to the interface with the surrounding capping layer and in the underlayer (UL). A Ge enrichment of the UL occurs as the temperature increases, accompanied by a Te depletion in the same area. This depletion is correlated with a Te enrichment right above the UL, in the bottom part of the GGST cell. The quantification of Te-rich regions yields a Te/Sb ratio of 0.37, very close to the expected value of 0.4 for GST. A deeper analysis of the elemental maps was made by extracting the composition from every pixel and plotting the Sb/Te, Sb/Ge and Te/Ge ratios. The composition tends to evolve into two opposite directions: Ge enrichment suggesting the formation of Ge grains, and Te-rich regions suggesting the formation of GST when compared to the theoretical ratios. The first crystallization events are observed at 350°C during *in situ* HRTEM experiments. HRTEM analysis after heating at 400°C reveals a complete crystallization of the various investigated cells. The Fast Fourier transforms calculated from HRTEM images were generated and combined with radial integration profiles to identify the different crystalline phases in presence (Fig. 1D). The analysis of the diffraction peaks reveals the presence of the Ge cubic and the GST metastable cubic phases. GST reflections appear at 390°C, highlighting two crystallization temperatures: 350°C for Ge, and 390°C for GST. These temperatures indicate that Te-Ge interdiffusion starts before the crystallization of the first Ge grains. By selecting all the reflections of each phase in the Fourier spectra of the experimental HRTEM images, numerical dark field images are produced, which allow mapping the various crystallized phases, and evidencing the crystallization of the Ge and GST nanograins mainly in the bottom part of the cell (Fig. 1C). *In situ* 4D-STEM analysis coupled with STEM-EDX acquisition are in development to perform both structural and chemical investigations simultaneously. These results, together with synchrotron XRD performed *in situ* during thin films crystallization [3], allow for a complete picture of the crystallization pathways of this Ge-rich GST alloy including elemental separation, crystallization and ordering of different phases, as well as texture in relation with various interfaces.

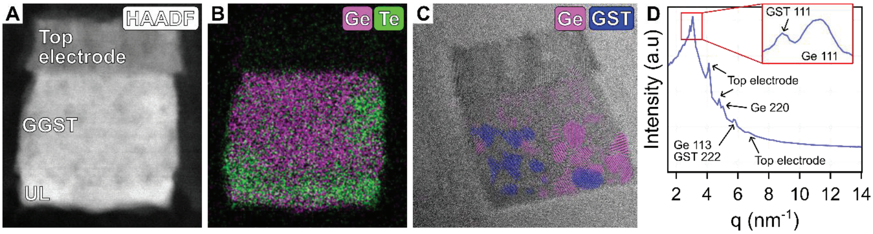

**Fig. 1** (A) STEM-HAADF image of a representative GGST cell with (B) its elemental map showing Ge, Sb and Te after a thermal pulse at 380°C. (C) HRTEM image of another GGST cell heated at 400°C, showing evidence of Ge and GST cubic phases inside the cell. (D) Radial integration profile of the corresponding FFT of (C) used to identify the different phases.

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# A Novel Thermally Stable Ruthenium Precursor Enabling Dense, Lower Resistivity and Inherent Selectivity against $SiO_2$ via Atomic Layer Deposition for Advanced Interconnects

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Ruthenium (Ru) has been widely investigated in the inteconnect metallization as a alternative candidate for replacing Copper (Cu), due to the reliability concerns of Cu such as electromigration (EM) resistance and time-dependent dielectric breakdown at especially scaled metal pitch. Ru is particularly promising due to its low resistivity with short electron mean free paths, high melting point, and chemical stability as a noble metal. It has high EM resistance inherently and does not require a diffusion barrier layer to prevent the diffusion into the surrounding dielectrics unlike Cu, making it suitable for advanced interconnect applications to overcome the miniaturization challenges. [1]

Atomic layer deposition (ALD) process can provide high-purity films with lower resistivity excellent step coverage in high-aspect-ratio structures and precise control over film thickness at the atomic scale due to its self-limiting surface reactions. ALD-Ru processes with $O_2$ as a co-reactant have been well examined and summarized with their various growth kinetics and thin film properties. The use of conventional high-valence precursors often suffers from a low growth per cycle (GPC). On the other hand, zero-valent Ru precursors also suffer from a relatively high resistivity mainly attributed to the poor thermal stability of the precursors (typically < 300 $^{o}$C) to hinder a higher temperature deposition, although they show high GPCs and shorter incubation cycles. [2]

Since both high GPC with self-limiting behavior and better film quality are essential for the desired ALD process, we have developed a novel heteroleptic Ru precursor, which has two small and simple molecular structure ligands, trimethylenemethane (TMM) and isopropylmethylbenzene (*p*-cymene). This precursor, [Ru(TMM)(*p*-cymene), synthesized at TANAKA PRECIOUS METAL TECHNOLOGIES Co., Ltd., Japan] shows a high thermal stability, no thermal self-decomposition up to 400 $^{o}$C. Self-limiting growth behavior at 300 $^{o}$C deposition was confirmed, corresponding to the excellent step coverage (>95%) on the trench wafer with aspect ratio ~4 (Figure.1). The GPC exhibits as high as 1.27 Å cycle$^{-1}$ when using $O_2$ molecules as a reactant. Incubation periods on metallic substrates show relatively short (~8 cycles on TiN), while surprisingly extended incubation periods >1000 cycles were observed on $SiO_2$. It indicates that an inherent selective deposition made possible by this novel Ru precursor, facilitating the specific application of Ru interconnect metallization, for example, bottom-up metal filling in scaled vias. (Figure. 2)

The deposited film shows better qualities, large grain sizes and lower impurities by virtue of high process temperature, leading to lower resistivity as ~14.2 $\mu\Omega$ cm (300 $^{o}$C, ~25 nm-thick Ru). The resistivity is still relatively maintained with the low value even at thinner thickness, being superior to the previously report about conventional Cu/TaN system for the reference [3] at < 10 nm when considering the thickness of diffusion barrier (TaN). Crystallographic analysis combined with Fuchs-Sondheimer-Mayadas-Shatzkes (FS-MS) modelling revealed that well enlarged crystallite and promoting the formation of coincidence site lattice (CSL), which is 3D superlattice facing two crystals with shared atoms to a specific orientation, are greatly attributed to mitigating grain boundary scattering, enabling as low as 10.6 $\mu\Omega$ cm (350 $^{o}$C, ~34 nm-thick Ru) without post-annealing (Figure.3). These unique features and new findings using a novel Ru precursor will offer the further possibility of Ru metallization for advanced interconnects.

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## Acknowledgments

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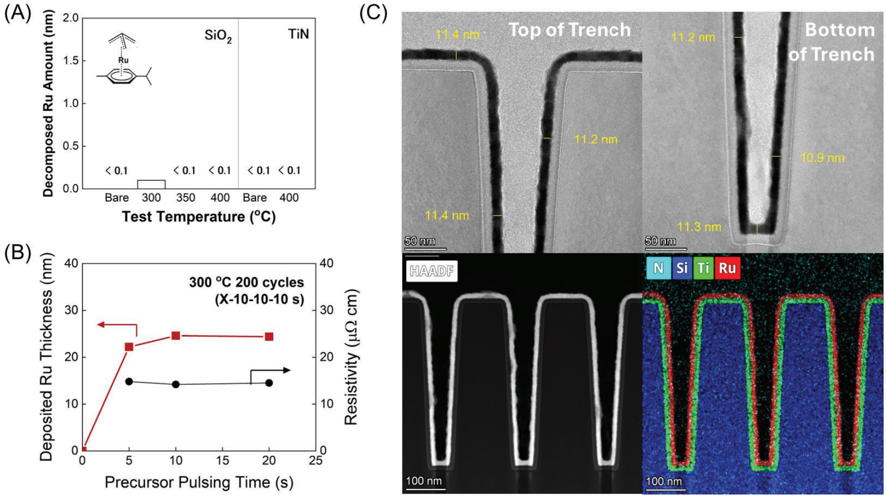

Figure 1. (A) Chemical structure of a novel Ru precursor [Ru(TMM)(*p*-cycme)] and its thermal stability evaluated by XRF where only the precursor was supplied into the ALD chamber without any reactants for 10 min. (B) Deposited Ru thickness by SEM and the resistivity of these thin films as a function of precursor pulsing time at 300 °C $O_2$ ALD with 200 cycles. (C) Cross-sectional TEM images at 300 °C deposition on TiN deposited trench wafer with aspect ratio ~4 (Top width: ~115 nm, Bottom width: 65 nm, Trench depth: ~415 nm), HAADF image (lower left) and elemental mapping quantification for full Ru, Ti, Si and N (lower right).

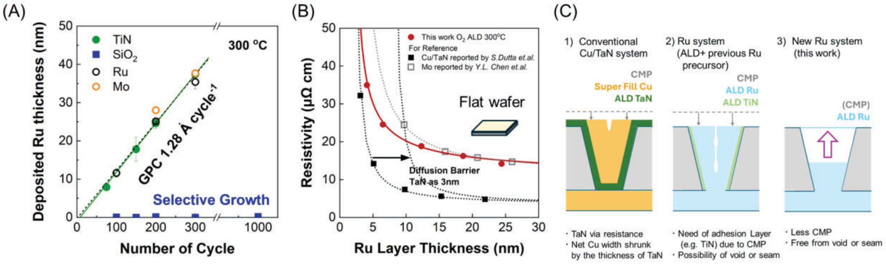

Figure 2. (A) The thickness of the ALD-Ru thin films deposited under optimized pulsing conditions as a function of the number of ALD cycles on TiN, $SiO_2$, Ru and Mo substrates. (B) Resistivity of deposited ALD-Ru and other metal (Cu, Mo; refs [3], [4]) thin films on flat wafer at 300 °C deposition (C) Schematic comparison images of via fabrication in the case of 1) conventional Cu/TaN system by superfilling technique for Cu and ALD for TaN, 2) Ru system by ALD using previous Ru precursor, 3) New Ru system by ALD using [Ru(TMM)(*p*-cymene)].

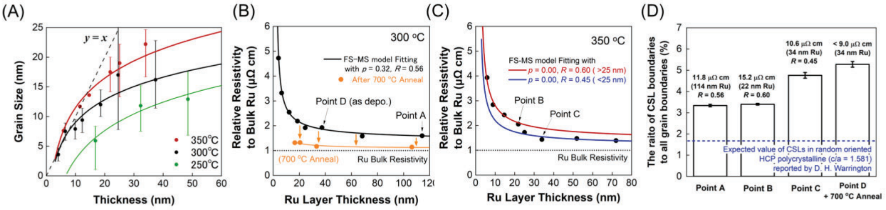

Figure 3. (A) Grain size derived from full width at half maximum of X-ray diffraction peaks using Scherrer formula at 250, 300, 350 °C. FS-MS modeling at a deposition temperature of (B) 300 °C, (C) 350 °C. (D) The relation between grain boundary scattering coefficient *R* and CSL ratio to all grain boundaries with ref [5].

# Underlayer selection for TiSiN ALD deposition on copper thin film

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## 1. Introduction

In the semiconductor industry there is a major drive to integrate ALD deposition in back-end-of-line (BEOL) applications, as it comes with substantial deposition benefits, such as near perfect conformity, homogeneous film structure and composition. These characteristics enable higher compacity of integrations. TiSiN is a promising material for BEOL applications due to its good copper barrier properties [1]. However, commercially available thermal ALD process of TiSiN is slightly above 400°C. At these temperatures, exposed copper layers tend to produce surface defects, commonly known as hillocks [2]. The aim of this work is to evaluate the morphological performance of a capping layer on exposed copper before TiSiN ALD metallization: an underlayer (UL).

## 2. Methods

Within this work 4 stacks were evaluated: a reference and three different metal underlayer (room temperature Ta PVD / 350°C W PVD / 400°C TiN CVD) were integrated on 300mm silicon blanket wafers, between a Ta barrier + 90nm Cu PVD layer and a 12nm 440°C TiSiN tALD layer. A short airbreak tool place between depositions on each wafer. High resolution XTEM (JEOL NEOARM 200kV) was conducted to observe the interfaces.

## 3. Morphological analysis

The experimental results are the following, Fig. 1: (a) No UL: High copper roughness and hillock formation, no intermixing between layers, (e) TiSiN crystallinity at copper interface, segregation of elements at interface, no TiSiN oxidation on either side. (b) Ta UL: No copper roughness, no intermixing, underlayer oxidation, crystalline Ta UL, amorphous Ta(O) and TiSiN. (c) TiN UL: Medium copper roughness, (k) intermixing with copper and TiSiN, (g) crystalline TiN with an amount of intermetallic formation. (d) W UL: copper oxidation, medium copper roughness, no intermixing, slight underlayer oxidation, (h) crystalline W and amorphous TiSiN layer.

Firstly, in the Fig.1 (a), as expected, direct high temperature TiSiN deposition induces Cu roughness and even causes the formation of hillocks. Secondly, in Fig.1 (c)/(d) The 'faster' PVD and CVD in temperature only induce grain movement and local roughness, with the 'cold' Ta(N) PVD being almost perfectly flat, Fig.1 (b). Due to airbreaks most processes exhibit interface oxidation and/or degradation, apart from TiN CVD UL, which intermixes with the copper on one side, and TiSiN on the other. Here, TiSiN tends to stabilize as an amorphous layer, its crystallinity on copper is hypothesized to be caused by different stoichiometry within the first layers.

UL deposition in temperature induces slight roughness, only room temperature deposition leaves a flat copper interface. Material-wise, tantalum or tungsten are presenting good barrier morphologies, whereas TiN CVD intermixing on either side does not demonstrate real separation.

The oxidation of interfaces could be prevented by integrating a copper reduction process before UL deposition, as well as TiSiN capping without airbreak.

## 4. Conclusions

The interfaces between TiSiN, Copper and three underlayers were evaluated by HR XTEM. The morphological analysis exposes severe interface degradation as well as copper movement for TiSiN ALD deposition without an underlayer. Several interface defects can be observed for each above shown tested condition, with each its drawbacks. The combination of materials and process temperature indicates that a low temperature deposition of tantalum or tungsten would make an ideal underlayer.

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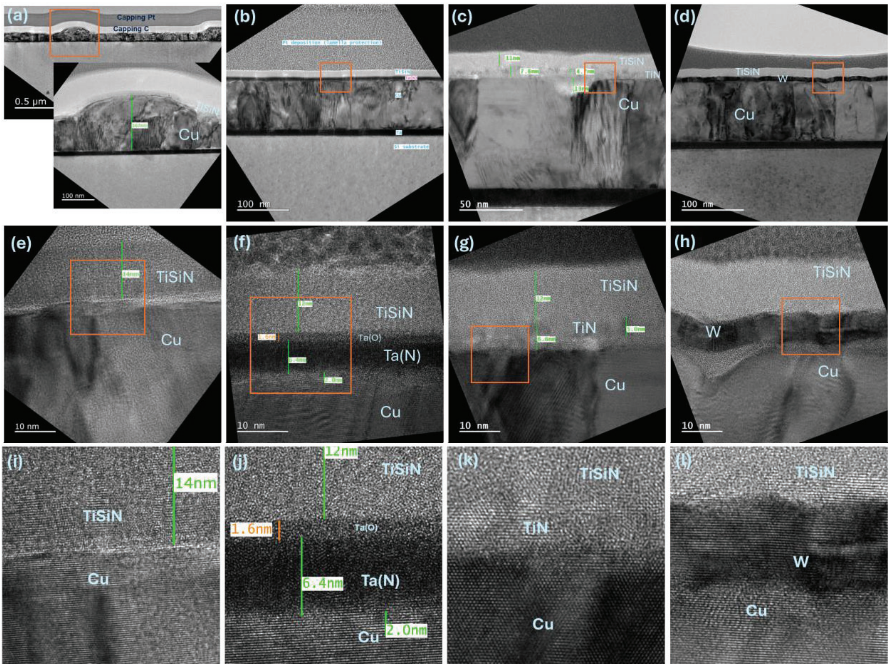

Fig. 1: Bright field high resolution TEM images of four stacks - (a)/(e)/(i) Cu PVD + TiSiN ALD – (b)/(f)/(j) Cu PVD + Ta(N) PVD + TiSiN PVD – (c)/(g)/(k) Cu PVD + TiN CVD + TiSiN ALD – (d)/(h)/(l) Cu PVD+ W PVD+ TiSiN ALD

# Ion Beam-Based 3D Nanopatterning for Multilayer and Micro-Optical Devices

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Nanodevice manufacturing will be faced with new challenges in future applications like quantum computing and/or integrated electro-optical devices for Photonic Integrated Circuits (PIC), such as:

- Processing and patterning of materials that are not used in standard microelectronics applications so far, and
- Generation of localized 3D structures.

Ion-beam etching is a versatile technique that meets the requirements for fabricating 3D nanodevices. Due to its high kinetic energy, ion beam milling (IBM) can pattern all materials through physical sputtering, eliminating the need for specific process chemistry. However, reactive ion beam etching (RIBE) may offer additional benefits, such as increased removal rate or improved selectivity. Furthermore, the anisotropic removal effect at low divergence enables ion-beam technologies to generate three-dimensional nanostructures.

The presentation covers specific applications of ion beam technologies in nanodevice manufacturing.

(1) Ion beam patterning of multilayer-based devices, e.g., tunnelling magnetics resistance (TMR) sensors:

The multilayer composition of the TMR sensor poses issues with the necessary etching required for electrical contacting. Classical dry-etching methods are limited due to the generally poor reactivity of magnetic materials. Additionally, the reactive gas required, such as chlorine, can cause corrosion of the sensor electrodes while in operation. The ion beam milling process uses noble gas ion bombardment to physically remove all materials used in the TMR stack. The ion beam source enables precise tuning of both, the ion density, and the ion energy. Additionally, dry etching with an inert gas, such as argon, voids any corrosion effects that can increase metal resistivity, hence destruct the sensor devices. The so called helium-backside wafer cooling is applied to keep the wafer temperature low enough enabling photoresist processing without resist damage.
Since the ion flux is well determined in terms of energy, energy distribution and directionality, one can achieve well-controlled vertical sidewalls, even in multilayers of various materials. Redeposition on the sidewalls can be counteracted by multi-step etching. This can help to avoid short circuits over thin isolating layers (Fig. 1)
The progress of the sputter etching process can easily be monitored using endpoint detection methods such as secondary ion mass spectrometry (SIMS) or optical emission spectroscopy (OES) (Fig. 2). These in situ diagnostics are indispensable when exact stop or switch points in the process must be met. Examples of the successful application of these techniques will be presented.

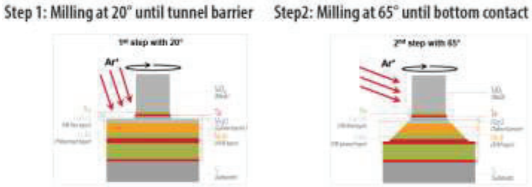

*Fig.1: Ion beam etching of TMR stacks at different angles*

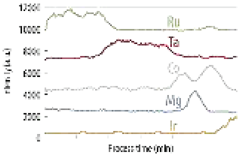

*Fig. 2: SIMS scan over time during IBM of a TMR stack*

(2) Generation of 3D structures in micro-optical devices:

Sidewall angles of optical devices often need to be adjusted to a defined slope. Even more complex 3D structures are employed in micro-optical devices, such as diffraction gratings and coupling grids. Because of the directional removal of an ion beam, the exact angular orientation of structures can easily be adjusted. For example, a ion-beam process will be used to produce slanted surface relief gratings (SRG) for use as coupling grids in data projection for augmented reality glasses.

Reactive ion beam etching (RIBE) offers unique process advantages to produce SRGs. Slanted structures with a strong defined undercut can be etched, a unique capability of RIBE. Crucial parameters for the RIBE process are selectivity between the mask and the substrate, and control of the geometry between the side wall angle and the bottom angle. By using different chlorinate or fluorinated etching gas mixtures, isotropic as well as anisotropic etching behaviour can be controlled, thereby defining the resulting geometry of the gratings. The ability to independently control ion energy and ion current is also used to adjust the slant shape and selectivity.

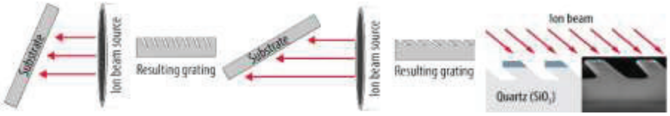

*Fig. 3: Ion beam etching of SRGs under different angles of incidence*

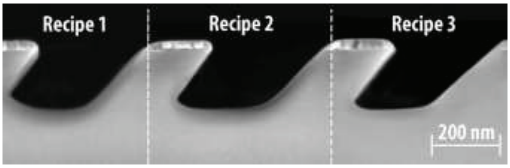

*Fig. 4: Isotropic and anisotropic etching by variation of reactive gases, ion energy, and ion current density*

Furthermore, this presentation will highlight how ion beam processing is used to produce waveguides for Photonic Integrated Circuits (PICs), providing the accuracy, consistency, and flexibility required for next-generation devices.

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# GaAs pin diodes – highly efficient and simple power devices

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Over the past decades, gallium arsenide (GaAs) has become an established material in high-frequency and optoelectronic applications and is, after silicon, the second most widely used material in the semiconductor industry [1]. Owing to its widespread availability, GaAs provides the foundation for the development of cost-effective, highly efficient pin diodes presented in this work, which represent an excellent alternative to SiC- and GaN-based power devices. The semi-wide bandgap material GaAs have not been taken into the consideration to design bipolar power devices like diodes and IGBTs for high voltage classes so far. Formerly, the potential of the GaAs based pin diodes were demonstrated in many literatures [2]–[6] for voltage classes of up to 600 V. GaAs material possesses many useful properties like high electron mobility in comparison to Si and SiC, twice the critical field strength as for Si, low intrinsic carrier density and low inherent minority carrier lifetime [7]

The presented work will summarise the latest developments in regard to utilize the inherent and beneficial material properties of GaAs combined with advanced manufacturing processes of an up to 100 µm thick epi-layer stack. The fabrication of vertical GaAs pin-diodes was done by metal-organic chemical vapor deposition (MOCVD) growing $n^{++}$ and $p^{-}$ epi-layer on 4” $p^{+}$ substrate with an overall epi thickness of up to 100 µm. The lateral junction termination is done by wet chemical etching down to the substrate and combined with new vertical surface passivation is introduced. The reliability data for those improved devices are presented for the first time.

The devices blocking voltages exceeding 1200 V and operate over a wide temperature range of up to 175 °C, while maintaining a low forward voltage drop for rated currents from 10 A to 60 A, as example see Fig. 1. Furthermore, ion irradiation offers the possibility to tailor the switching behavior according to specific application requirements. The reduction of the charge carrier lifetime through the introduction of deliberately engineered defects results in a substantial decrease in reverse recovery charge during switching events, thereby enabling significantly lower switching losses. The device development is supported by simulations using SILVACO TCAD [8], showing the that the reverse recovery charge was reduced from 1880 nC to 380 nC for the simulated, as well as for the fabricated diodes, with tailored lifetime. The GaAs diode with lifetime killing shows nearly 5 times reduction in $Q_{rr}$ than the diode without lifetime reduction. The reverse recovery maximum current ($I_{rrm}$) got reduced from 38 A to 17.5 A for such improved diodes, see Fig. 2.

A typical application of such diodes is the phase-shifted full-bridge (PSFB) topology. In the 10 kW power class, performance comparable to SiC-based solutions was demonstrated [9], see Fig. 3 (a). In addition, when applied in a boost converter, a significant efficiency improvement was achieved, particularly under partial-load conditions, see Fig. 3 (b). Overall the GaAs diodes are ideal for soft switching topologies (LLC, PFSB etc) and secondary side rectification applications like industrial battery charging, welding, induction heating and much more.

In combination with mass production costs are significant lower as SiC, GaAs pin diodes could be proven as suitable candidate for high efficient application replacing Si, SiC and GaN power devices.

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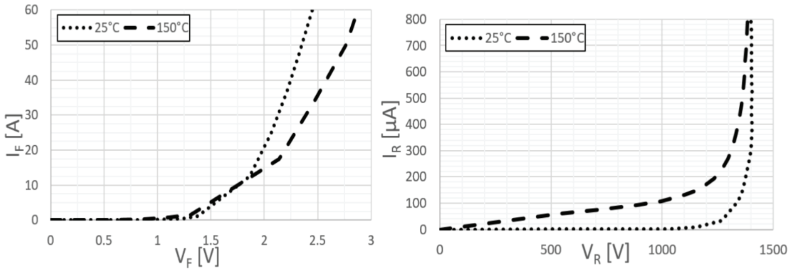


*a)* *b)*

Fig. 1: Exemplaric forward (a) and reverse (b) characteristic of a soft switching 60 A, 1200 V GaAs pin diode at 25 °C and 150 °C.

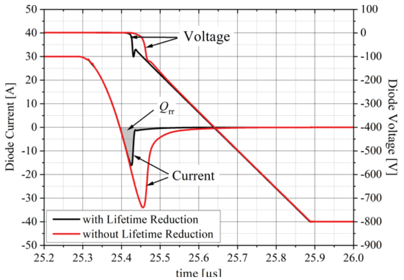
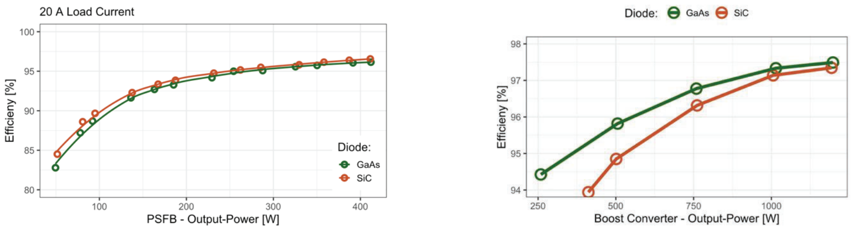


Fig. 2 Simulation of the dynamic behavior for GaAs pin diode with and without lifetime reduction at 300 K, 30 A, 500 A/µs, and 800 V DC-link voltage.



*a)* *b)*

Fig. 3: Efficiency comparison between GaAs and SiC devices in a soft-switching converter at a load current of (a) 20 A and a maximum output power of 8.2 kW at 100 kHz, adapted from [1]. Silicon hyperfast diodes experienced thermal failure at load currents exceeding 10 A and are therefore not included. In (b), a comparison of the efficiency of a SiC Schottky diode and a GaAs pin diode from 3-5 Power Electronics GmbH in a boost converter (PFC) operating at a switching frequency of 100 kHz.

# TMD Superlattices for Phase Change Memory: Growth and Thermal Characterization

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## Introduction

Superlattices are mainly studied for use in phase change memory, because their nanolaminate structures allow for heat confinement, lower switching energies while also preventing resistance drift [1]. From a broader perspective, superlattices are a playground for material properties, especially when considering thermal conductivity.

## Material Choice and Growth

Transition metal dichalcogenides (TMDs) encompass a broad set of materials with a large array of properties. A subset of TMDs are studied as candidates to be used in PCM superlattices. Their structure, consisting of 2D sheets separated by Van der Waals gaps make them compatible with van-der-Waals gap bound phase change materials like $Sb_2Te_3$. A selection of 9 TMDs is studied, all from the 3 by 3 element grid between titanium and tungsten. These metals are predicted to have a $M\mathrm{Te}_2$ crystal structure resembling $CdI_2$. The growth of these materials is performed through magnetron sputtering from elementary pure targets. In order to create the correct stoichiometry, the sputtering power of each target is individually tuned, while the sample is rotate through the flux of the two material. This method resembles the method of modulated reactants [2]. The materials deposited through this method crystallize in the $CdI_2$ structure after anneal, with some materials already crystalline upon deposition. The $CdI_2$ structure with texture of the 00L plane parallel to the substrate is evident from the XRD patterns in Fig. 1. The texture of these materials is further substantiated by rocking curve analysis.

## Thermal Conductivity

When heat, intended to drive the phase change, diffuses into the surroundings, this is detrimental for the power consumption of the device. Typical phase change materials, such as $Sb_2Te_3$, GST and GeTe typically demonstrate not only a high thermal conductivity, but also a high contrast between amorphous and crystalline state. Superlattices prevent this by lowering the cross-plane thermal conductivity. This can be measured through time-domain thermoreflectance (TDTR). Using TDTR, the TMDs are studied individually before studying them in a superlattice. At room temperature, the intrinsic thermal conductivity is extracted, as shown in Fig. 2, leading to a broad spread of values. The superlattices, however, all demonstrate a low thermal conductivity, both in as-deposited as well as in crystalline phase.

## Optothermal Cycling

Phase change material performance is typically quantified through electrical devices. Although this method is very application-relevant, results are typically heavily dependent on device parameters. In order to get a more device-independent metric, a laser based method is presented. Fig. 3 shows an example of repeatable switching that was obtained with this method on a $Sb_2Te_3$ thin film. The beam and scanning electronics of a confocal microscope are used to locally heat the phase change material. By tuning the parameters, both crystallization as well as amorphization are possible, in a process called optothermal cycling [3].

## Conclusions

Sb2Te3/TMD superlattices are studied. Deposition of the TMDs is done through magnetron sputtering through a method resembling the method of modulated reactants. Thermal conductivity measurements show that metal choice is important for the high-temperature behaviour of the superlattices. At room temperature, the interfaces in the system dominate the thermal resistance. Optothermal cycling is presented as a more fundamental, device independent method of functional characterization.

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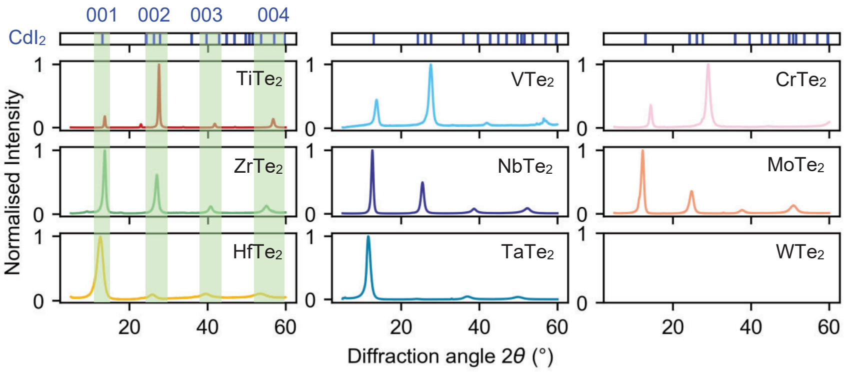

**Figure 1.** XRD results for deposited $M\mathrm{Te}_2$ films with $M$ one of the elements in the 3 by 3 grid between Ti and W. All but $WTe_2$ crystallize into the CdI structure with 00L planes parallel to the substrate after anneal.

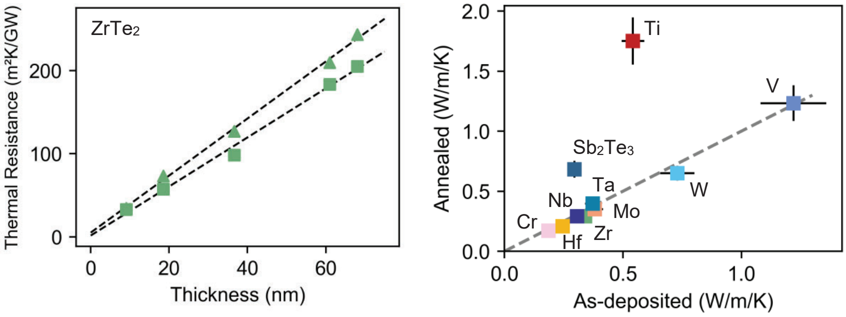

**Figure 2 (left)** By depositing a thickness series, the intrinsic thermal conductivity of a material is measured. The thermal resistance because of the interfaces in the system can be calculated through extrapolation. **(right)** The room temperature thermal conductivities of all studied TMDs, only the metal is noted for clarity. The dotted line signifies no contrast between the as-deposited and amorphous state. Most TMDs lie in the lower left corner, signifying a low thermal conductivity.

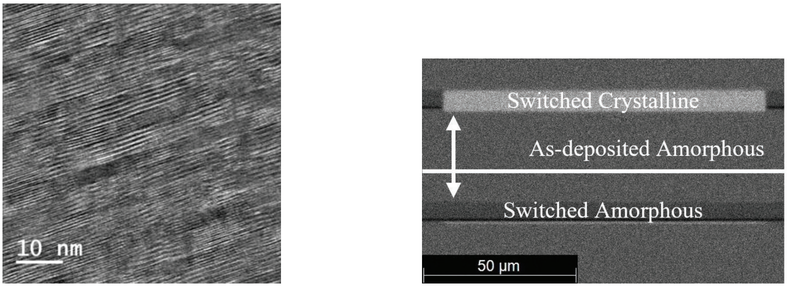

**Figure 3 (left)** A high resolution TEM micrograph of an annealed $TiTe_2$/Sb2Te$_3$ superlattice shows the highly textured nature of both materials. There is a clear preferred orientation parallel to the substrate. **(right)** Optothermal switching results for a $Sb_2Te_3$ thin film. Through this method, the material can consistently be switched between the two states.

# Simulation of Si Epitaxy in Single Wafer Reactors

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Silicon epitaxy (EPI) is an important process in semiconductor industry. We investigate Si epitaxy using 3D reactor scale computational fluid dynamics simulations coupled with surface chemistry models for the film growth.

In the first part we focus on the deposition of Si and phosphorous-doped Si at low temperature in a simplified reactor geometry. Based on existing DCS-based Si chemistry models [1] for higher process temperatures, we developed a new kinetic chemistry model for lower temperatures [2]. These chemistry models are coupled with CFD based simulations for the gas transport and multi-component diffusion of gas species using the software CFD-ACE+ [3]. This allows for reactor scale process simulations to get a better understanding of the relations between deposited rates and process parameters, enabling rational process optimization, to reduce process variability and to increase within-wafer growth rate homogeneity.

In the second part we introduce our ongoing work on developing a model for a high temperature atmospheric pressure Si epitaxy process using trichlorosilane. Here we investigate the flow field and gas species distribution in a complex 3D reactor geometry using the software COMSOL Multiphysics [4]. The gas mixture consists of hydrogen ($H_2$) and trichlorosilane (TCS, $SiHCl_3$) with a spatially varying concentration above the rotating wafer. Simulating and visualising the 3D flow field (see Fig. 1) and gas composition is the first step towards an in-depth understanding of the process and optimising it for better homogeneity of the grown layer thickness. We are currently adding radiative, convective and conductive heat transport and we plan to include surface chemistry in the future. This will result in a complete multiphysical model – a digital twin – of this Si-EPI process.

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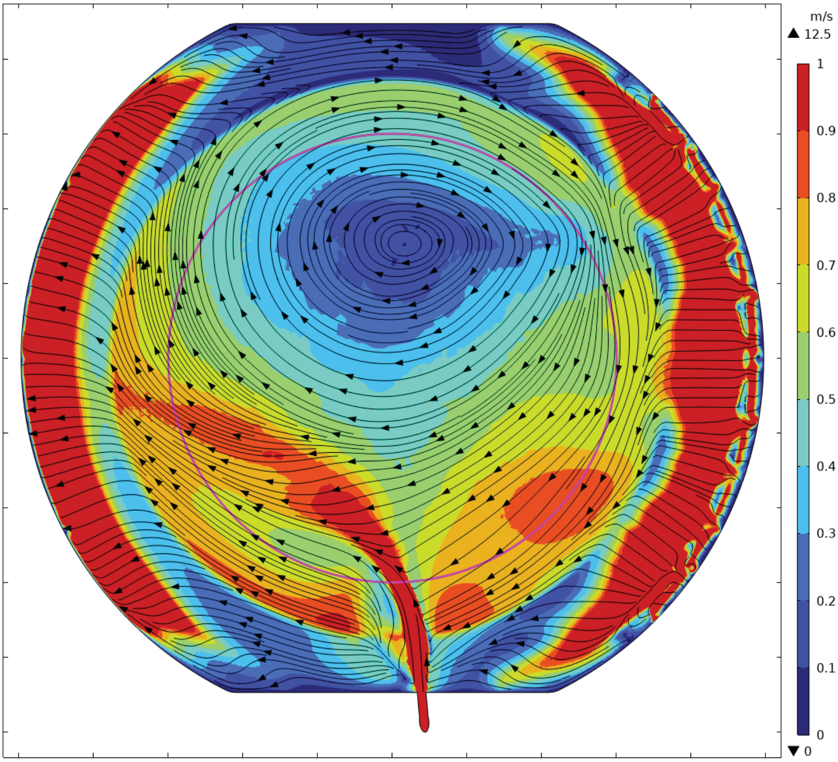

**Fig. 1:** Gas velocity distribution above a rotating wafer in an atmospheric pressure silicon epitaxy chamber with crossflow using $H_2$ and TCS.

# Laser-Based Annealing of Nickel Contacts for SiC Devices: Towards Thermally Robust Power Interfaces in 3D-Integration

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Thermal management and electrical integrity pose significant challenges in 2.5D and 3D packaging, particularly for wide-bandgap semiconductors such as silicon carbide (SiC), which enable advanced, power-dense systems in automotive and high-performance computing applications. Consequently, Ohmic contact formation (OCF) for SiC must advance beyond traditional rapid thermal processing (RTP) to address the requirements of thinner substrates, lower thermal budgets, and increased integration density.

This study investigates a laser-based method for localized OCF on SiC, utilizing diode-pumped solid-state lasers (DPSSLs) at ultraviolet wavelengths. The effects of laser fluence, pulse duration, and beam overlap on the formation of nickel silicide (NixSiy) contacts on 350 µm-thick 4H-SiC wafers with 70 nm NiAl metallization are systematically examined. Qualitative process trends are established using structural, electrical, and chemical performance indicators, with particular attention to the suppression of carbon-rich interfacial layers, which are critical for interface reliability under elevated thermal and electrical stress.

The principal findings of this investigation are summarized as follows:
(1) Laser-based Ohmic contact formation enables electrically stable contacts at high laser fluences, demonstrating both robustness and process tolerance;
(2) Laser energy density predictably determines the thickness and uniformity of nickel silicide (NixSiy) layers;
(3) Reducing pulse overlap to below 30% minimizes carbon accumulation at the metal/SiC interface.

This laser-driven technique offers a promising alternative to RTP, especially for localized processing and reduced thermal budgets. By minimizing global substrate heating and enhancing interface stability, this approach improves thermal integration compatibility for SiC-based power devices in 2.5D and 3D packaging environments.

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# Atomic Layer Deposition of Titanium Oxide for Integrated Applications

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Titanium oxide is a material of recent interest for various applications. Especially the high refractive index of $TiO_2$ of 2.4 at 633 nm [1] enables $TiO_2$ as material of choice for surface relief grating structures. However, the fabrication of nano-scale $TiO_2$-based gratings is accompanied by various challenges. Haase et al. demonstrated the technological integration via nano-imprint lithography and subsequent dry etching. [2] Alternatively, a double patterning approach overcomes these challenges.

Another relevant property of $TiO_2$ is its high relative permittivity ranging from 16 to 100. [3] This makes $TiO_2$ an interesting material for storage applications as in MIM (metal insulator metal) or MIS (metal insulator semiconductor) capacitors. The low band gap of the material – and in consequence the low breakdown resistance – can be addressed by the combination of $TiO_2$ with another dielectric material with higher band gap, such as $Al_2O_3$. [3,4]

This material combination is further an excellent material stack for moisture barrier layers. Both materials, $Al_2O_3$ and $TiO_2$, are quite inert and won't be affected by external moisture influence. Multi-layer stacks are used to encapsulate quantum dots for example. [5]

All these mentioned applications require homogeneous coatings of a dense $TiO_2$ film in small dimensions and also in challenging geometries. This includes the coating of sidewalls of 3D structures within nanometre dimensions. The technology of choice for these applications is the atomic layer deposition (ALD). This deposition method separates the reactive species for the deposition and uses the surface adsorption of the precursor in order to create a self-limiting coating. This will be oxidised in a following step completing one single cycle. With increasing number of cycles, the film growths conformally on almost any geometry.

Within this work, we'll present the integration of ALD-based $TiO_2$ films for different applications. The process was developed by use of TDMAT (Tetrakis(dimethylamido)titanium) as precursor and ozone as oxidising agent.

We demonstrate the conformal coating of trench structures with an aspect ratio of 64:1. The trenches with a width of 500 nm – hard mask opening of 350 nm – and a depth of 32 µm had been coated with a $TiO_2$ film. (Figure 1). The film on top of the hard mask has a thickness of 20 nm. The vertical sidewalls on the top of the structure also contain a 20 nm thick film. Same film thickness could be achieved in the bottom of the structure (see Figure 1 lower right). The 3D integration ability has been used to fabricate free standing $TiO_2$ gratings. Figure 2 shows the final integration on a silicon substrate. These had been fabricated by coating a structured sacrificial $SiO_2$ layer with vertical sidewalls.

This coating of 3D structures is a key requirement to fabricate MIS and MIM capacitors. In order to optimise this the electrical performance of the ALD film was characterised (see Figure 3). Figure 3 a) shows the effective $\kappa$ value of the dielectric in the MIS structure. The baseline is $Al_2O_3$ with a value of 3.2. The amorphous $TiO_2$ film of 5 nm reaches a $\kappa$ value of 5.7 while the crystalline $TiO_2$ film of 10 nm reaches a $\kappa$ value of 10.4. The layer stack of 5 nm $Al_2O_3$ and 5 nm $TiO_2$ reaches an effective $\kappa$ value of 7.5, while the (10 + 10) nm layer stack reaches an effective $\kappa$ value of 9.9. $TiO_2$ is a semiconducting material and suffers a substantial leakage current due to its intrinsic conduction. A low bias of 0.1 V (20 MV/m) will lead to a leakage current density of $10^{-7}$ A/mm² in a 5 nm thin film. Increasing the film thickness to 10 nm will reduce the leakage current density – under the same electric field – to just $10^{-8}$ A/mm². In contrast, a 5 nm $Al_2O_3$ film has a way better performance as the leakage current density is in the order of $10^{-14}$ A/mm² for the same conditions. The combination of both films can achieve the low electrical leakage of $Al_2O_3$ in combination with the high $\kappa$ value of the $TiO_2$. This enables a high performative platform for device integration using high-capacity modules.

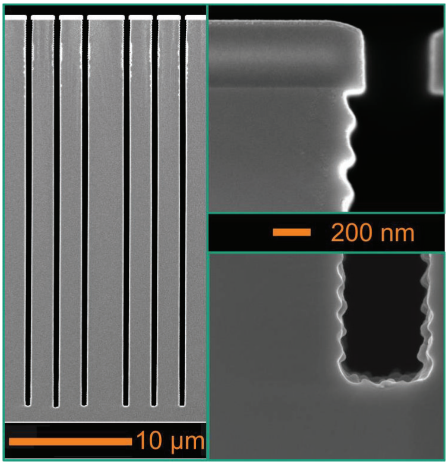

**Figure 1: Scanning electron microscope images of trench structures coated with $TiO_2$.**

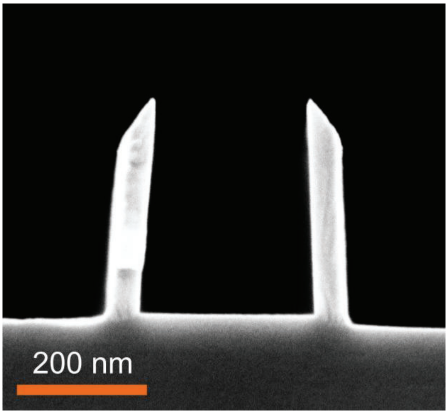

**Figure 2: Free standing $TiO_2$ grating structure.**

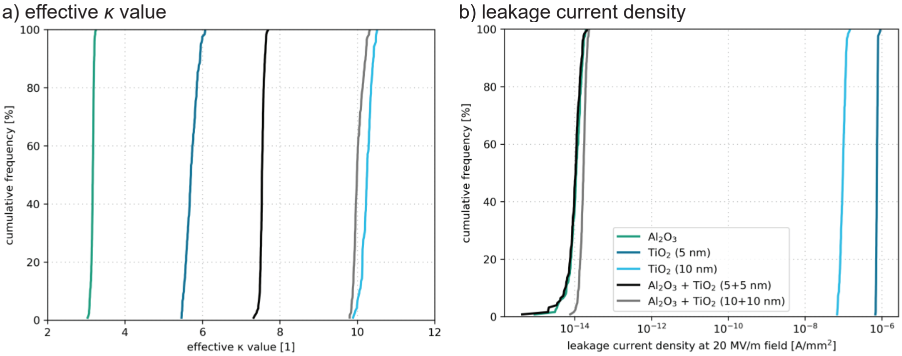

**Figure 3: Results of electrical measurements of different $TiO_2$ and $Al_2O_3$ films: a) effective *κ* value of the dielectric in a MIS structure, b) leakage current in the MIS structure under 20 MV/m electric field.**

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# Investigation of the oxidation and reduction behavior of thin copper surfaces in semiconductor technology

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During the processing of semiconductors, defects may occur and may cause yield or reliability issues. Filling voids in copper lines and/or vias are known and are a prominent defect type [1]. Figure 1 shows a transmission electron microscopy (TEM) image of such a void. Extensive investigation on the phenomena over the past years and decades using production-optimizing methods, revealed many influencing parameters and knobs to reduce the occurrence of the defects. But a proper solution to this issue has not been found. It is known that the transportation of wafers and its duration between the copper seed layer deposition and copper electroplating steps have a crucial influence on defect formation. Defects can be reliably introduced by storing or transporting wafers in open 200mm cassettes in the cleanroom for extended periods. The proposed defect mechanism behind this is thought to occur as follows: local oxidation of the copper seed layer prevents the plating process from initiating correctly, leading to overplating on adjacent surfaces.

This work aims to characterize the physiochemical processes occurring at the Cu surface. The experiments were conducted on 200mm blanket wafers using either a Ta or TaN/Ta barrier and a 30nm thin Cu seed layer. To this end, an ellipsometric model is developed, which can measure the thin copper oxide layer on top of the copper seed layer. The model was optimized using external measurements by time-of-flight spectrometry (ToF-SIMS) and X-ray photoelectron spectroscopy (XPS) on freshly prepared samples. Various storage conditions for the copper seed layer in a cleanroom environment were tested and compared. Also, a potential influence of different barrier systems is investigated.

The ellipsometric model confirms expectations from the literature showing a logarithmic growth rate of the oxide layer [2]. Moreover, the model verifies the reported order of magnitude of a few nanometres of oxide formation after several days of storage [3,4]. It was found that the thickness of the oxide layer depends strongly on the storage and transport conditions. Older storage conditions like open cassette storage, or storing in boxes, which provide protection from laminar cleanroom airflow, were compared to more modern methods like storage in front-opening unified pods (FOUPs), either unpurged or nitrogen purged. The lowest oxide formation was found for the storage in nitrogen purged FOUPs, leading to nearly no oxide formation. Figure 2 compares the growth rates found for different storage modes.

Additionally, the effectivity and stability of a diluted sulfuric acid step removing the copper oxide layer was investigated. However, a rapid re-oxidation of the surface is observed after successful reduction, occurring at a significantly faster rate than the initial oxidation (Fig. 3).

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Figure 1. TEM image of the fill defect in a copper via. Image taken after anneal and CMP.

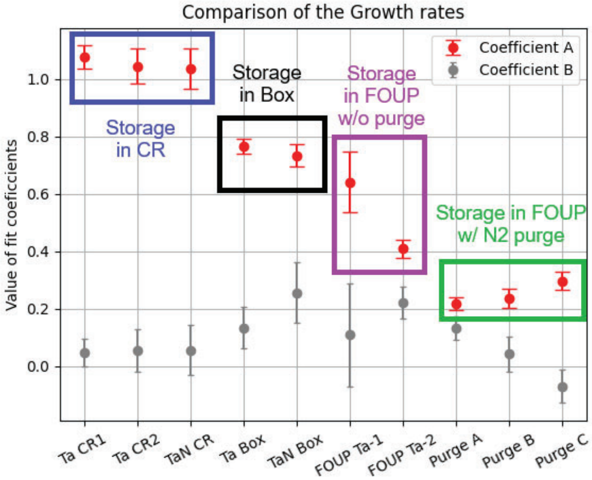

Figure 2. Comparison of growth rates for different modes of storage. The description codes Ta, TaN refer to a Ta or a Ta/TaN barrier underneath the seed layer. The abbreviation CR refers to cleanroom conditions, box means a 200mm transport box. A FOUP is a modern 300mm transport container. The fit function is *f(x)*=A**ln(x+1)*+B.

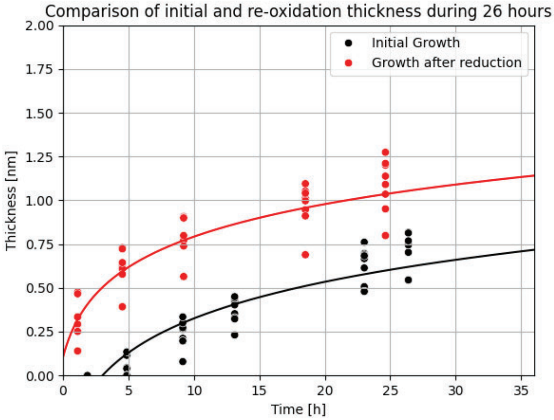

Figure 3. Comparison of re-oxidation after sulfuric acid treatment and initial oxidation during the first 26 hours. The wafers were stored in the clean room.

# Characterization of interactive forces between CMP pad and ILD materials depending on post CMP clean

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For copper metallization chemical mechanical polishing is necessary to enable damascene processing. After removal of copper overburden and barrier a defined amount of ILD material is removed to ensure isolation of all individual copper structures. The polishing process itself is necessarily followed by a dedicated cleaning step (PCC). For the PCC step various commercial cleaning chemistries are available that balance mainly particle removal and prevention of corrosion between copper and barrier material [1]. For the aspect of particle removal, it is necessary to evaluate impact of leftover particles on the final product to ensure a clean as gentle as possible. In case of particle residuals affecting the overall performance, techniques are needed to understand the root cause of the particles and act accordingly. A standard SEM review gives insights on the type of particles e.g. silica abrasive particles or organic pad residuals. Based on this, further methods are required to understand the particle wafer interaction.

Different levels of post CMP wafer surface defects were observed on various ILD materials. SEM review revealed the particles to be mainly pad debris. For improvements in PCC performance the attachment between ILD surface and pad debris needs to be measured. As particle wafer interactions depend strongly on the surrounding medium it is crucial to perform any measurements including the correct ambient e.g. liquid cleaning chemistry. One of the few measurement techniques offering data on particle surface interactions including liquids is AFM force measurement. However, the technique is commonly used only for fundamental science and depends highly on good sample material [2]. To apply the technique for investigation of semiconductor production challenges, it is critical to use the exact materials.

In this work we show defect level data on different standard BEOL ILD materials for 28 nm technology node post copper CMP (Figure 1). A clear trend in defectivity depending on the ILD material can be seen for data on 300 mm wafer size. Based on this, AFM force measurements in between coupons coated with the ILD material and CMP pad particles were carried out and will be presented. To achieve suitable particles of the specific CMP pad material for attachment of the AFM cantilever $LN_2$ milling was performed (Figure 3). Attraction force measurements were carried out including the PCC chemistry (Figure 4). This measurement setup enables us to access the interaction force data between production standard materials (both ILD and pad) in process identical medium (PCC chemistry).

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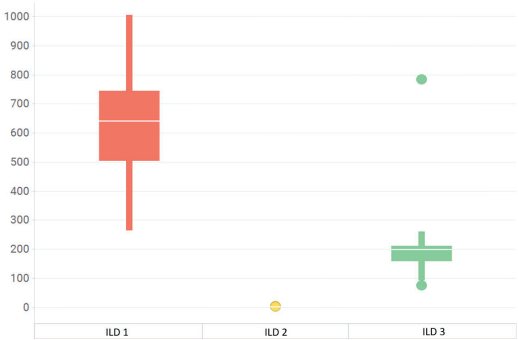

Figure 1: Defect level for different ILD materials after identical post CMP cleaning

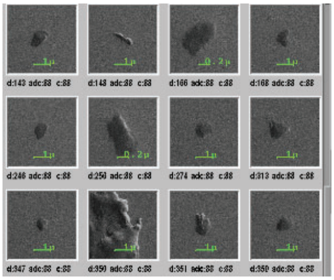

Figure 2: SEM review of defects on ILD material, showing pad debris

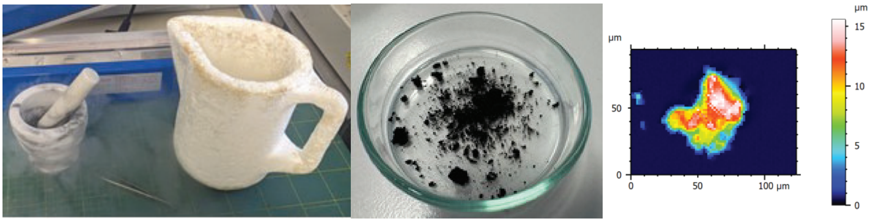

Figure 3: from left to right: LN2 milling of pad material; grinded pad material particles; confocal microscopy image of pad material particle

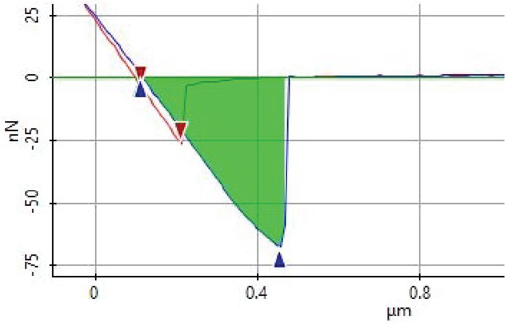

Figure 4: AFM force curve showing interaction of -70 nN between pad material and ILD

# Monitoring-Based Control and Process Interruptions Recovery Strategies for Slurry Residues in Serial CMP of IMD Oxides

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In advanced integrated circuit manufacturing with AlCu metal interconnects, the planarization of intermetal dielectric (IMD) oxides by serial CMP plays a critical role in determining final surface defectivity1. This defectivity directly impacts plug patterning quality, the adhesion of subsequent dielectric and metal layers, and ultimately device yield and reliability. Among the different process parameters, the choice of slurry can have a significant influence.

This work investigates a CMP scheme based on an elongated colloidal silica slurry containing 16% wt. dispersed particles, focusing on a specific defect type: slurry residues. The study is built around two main axes.

The first is the analysis of the impact of process interruptions within the serial CMP sequence on final surface defectivity, with particular reference to slurry residues on the oxide surface. Critical process steps and associated wait times were identified, beyond which slurry particles dry on the oxide surface. It was found that, once these critical times are exceeded under specific conditions, the resulting residues can no longer be completely removed by the subsequent cleaning step when the cleaning chemistry does not include diluted HF2.

The second axis concerns mitigation strategies. A monitoring and alarm system was developed to detect when the critical time window is reached or exceeded, together with a dedicated recovery procedure designed to restore surface quality at the end of the process, even in the presence of such interruptions.

The combined implementation of critical-time interception and the recovery flow enables the IMD surface to be maintained within planarity and cleanliness specifications compatible with robust plug definition and good adhesion of subsequent layers, thereby minimizing the impact on device yield and long-term reliability.

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**Figure 1.** Optical image of a slurry residue. Silica nano particles are visible on the surface

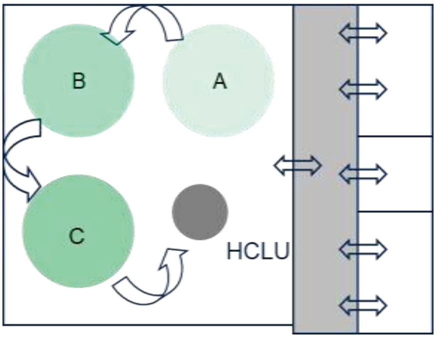
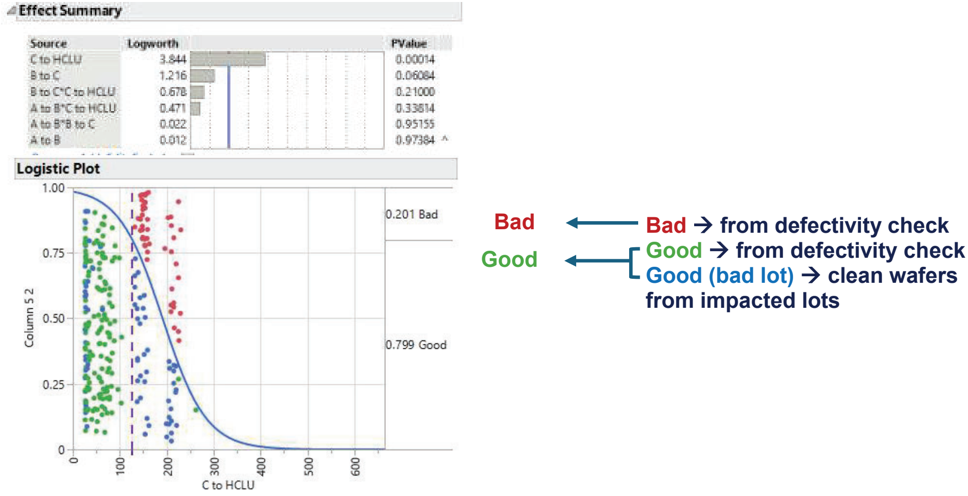


**Figure 2.** Serial CMP equipment scheme



Effect Summary

| Source | Logworth | PValue |
|---|---|---|
| C to HCLU | 3.844 | 0.00014 |
| B to C | 1.216 | 0.06084 |
| B to C*C to HCLU | 0.678 | 0.21000 |
| A to B*C to HCLU | 0.471 | 0.33814 |
| A to B*B to C | 0.022 | 0.95155 |
| A to B | 0.012 | 0.97384 |

**Bad** → **from defectivity check**
**Good** → **from defectivity check**
**Good (bad lot)** → **clean wafers from impacted lots**

**Figure 3.** Logistic plot and Summary Effect to correlate the main contributor on the critical waiting time during CMP process with defectivity results

# 300 mm CMOS Compatible ZrN based SC BEOL Demonstrator & Trench-Array Structures for Testing Via Superconductivity

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A superconducting back-end-of-line (SC-BEOL) is a key enabler for high-performance cryogenic electronics including Superconducting Quantum Computing control hardware and Single Flux Quantum (SFQ) digital circuits. Compared with conventional Cu BEOL technology, superconducting interconnects enable significantly higher clock frequencies while simultaneously reducing dissipative losses.

In this work, we present a 300 mm CMOS-compatible process for the fabrication of a superconducting BEOL demonstrator (Fig. 1) employing sputtered ZrN as the superconducting material and TEOS-based PECVD $SiO_2$ as the interlayer dielectric. The process flow is inspired by established SFQ process nodes by MIT Lincoln Laboratory [1] and imec's semi-damascene approach [2] and incorporates some non-standard integration features. First, ZrN patterning combines subtractive and additive approaches: metal layers are structured subtractively, whereas via layers are defined additively. Second, V1 and M2 are deposited within a single sputter step. As a consequence, hollow vias are formed in which ZrN is present only along the Via sidewalls.

Cryogenic four-point measurements in an OptiCool cryostat of a 2-Via structure confirm electrical connectivity through M1-V1-M2; however, the interconnects do not exhibit superconducting behavior. The absence of superconductivity is attributed either to (i) surface damage of M1 induced by the $SiO_2$ via etch or (ii) to a non-superconducting crystal structure of ZrN on the V1 sidewalls. For an isolated analysis of the potential influence of the altered V1 ZrN, trench-array test structures were fabricated. Arrays of 2x30 trenches with widths of 500 nm at 1:1 pitch were etched into $SiO_2$, followed by deposition of 50 nm ZrN (Fig. 2). For four-point measurements across the trench array, the measurement region was electrically isolated by milling a rectangular contour to a depth of approximately 200 nm using a $Ga^{3+}$-ion FIB (Fig. 3 & 4).
Two sample variants with trench depths of 50 nm and were evaluated at 2 K. Structures with 100 nm trench depth show purely resistive behavior below and above the critical current (Fig.5a). In contrast, the 50 nm trench depth structures exhibit superconductivity followed by a mixed regime which is characterized by resistive conduction and multiple voltage steps, and finally a transition to fully resistive behavior above the critical current (Fig.5b). The mixed regime is attributed to ZrN inhomogeneities within the trenches, causing spatially varying local critical currents and sequential loss of superconductivity.
These results indicate that geometry-dependent film properties critically influence superconducting via performance and must be tightly controlled for reliable SC-BEOL integration.

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Acknowledgment

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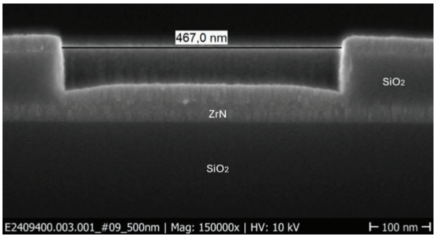

Fig.1: SEM X-Section of a ZrN based SC BEOL demonstrator with 100 nm etch depth.

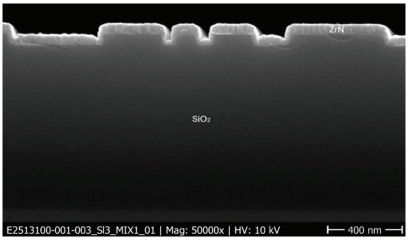

Fig.2: SEM X-Section of SEM-Bars of varying width and 50 nm etch depth.

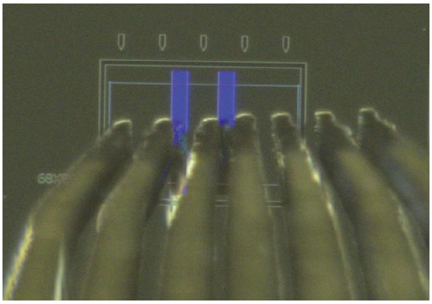

Fig.3: Four-point trench-array measurement setup with electrically isolated measurement area. The 2 × 30 trenches are identifiable by the blue coloration. The central probe is configured such that no current flows through it (I = 0 A).

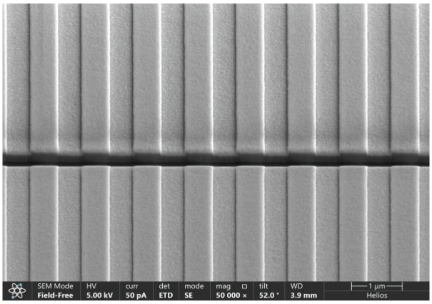

Fig.4: SEM micrograph of a 500 nm wide trench-array isolation cut produced by $Ga^{3+}$-ion FIB milling.

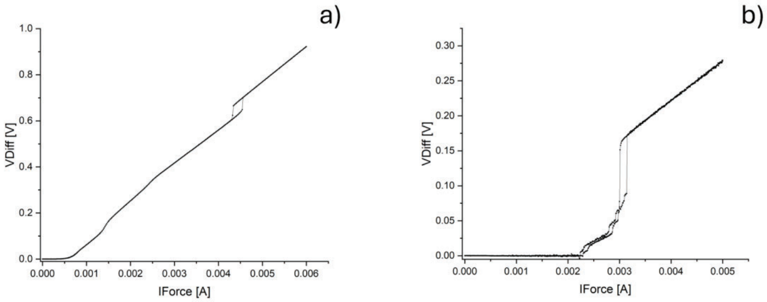

Fig.5: Four-point-IV-measurements of trench-array test structures with 500nm width at 1:1 pitch: a) 100 nm trench etch depth, b) 50 nm trench etch depth. IForce is swept in both directions.

# Plasma enhanced Atomic Layer Etching on AlGaN/GaN: process development, stability, recess etching of source, drain and gate

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Continuous device miniaturization necessitates etching techniques with exceptional precision and control. ALE is a key process technique enables precise, controllable etching with minimizing the structural damage and therefore enables new possibilities in device manufacturing [1]. The plasma ALE process consists of two independent steps forming a repeatable cycle. In the case of AlGaN etching, the first step involves chemical surface modification, achieved through halogenation using $Cl_2$ plasma. In the second step, the modified surface layer is removed by low energy Ar ion bombardment [1-8]. Typically purging in between the steps is applied, which increases the cycle time and affects the processing costs, too. A high degree of self-limitation in each step determines the controllability and stability of the process. Overall, the tool condition strongly impacts the EPC and self-limitation.

Atomic Layer Etching (ALE) has become increasingly important as a precise technique for AlGaN/GaN-based device fabrication, enabling highly controlled gate or contact recess etching. By recessing the barrier below the ohmic contacts, the contact resistance can be improved, which is beneficial for the overall Ron of the AlGaN/GaN HEMTs [9] and therefore decreases the switching losses and helps to exploit the full potential of those devices. With a controllable and low-damage gate recess the threshold voltage $V_{th}$ can be tuned and shifted even to positive values [10-15].

We will demonstrate that maintaining process reproducibility in ALE of AlGaN is challenging due to chamber wall contamination. Chlorine compounds deposited during modification steps can desorb into the argon removal plasma, disrupting self-limitation and altering EPC. Long operation can challenge chamber cleanliness and process reproducibility, making in-situ monitoring, such as optical emission spectroscopy, necessary. Chamber cleaning and conditioning procedure were established, and it will be demonstrated that they are critical for maintaining process repeatability and should be incorporated into process development.

As a second focus the cycle time was reduced to improve costs and sustainability of conventional ALE. Due to additional purging and evacuation sequences after each step, an ALE process lasts longer than a conventional reactive ion etching (RIE) process [16]. By minimizing or eliminating purge steps [16, 17] and optimizing plasma parameters or combining chemistry within one process step [18], cycle times can be reduced. For this reason, five ALE modifications were developed and compared: full-purge (1), half-purge (2), purge-free (3), continuous plasma (4) and bias pulsing (5). Their sequential structure over time is shown in Fig. 1a. Thereby the overall process time can be reduced by more than 60% while maintaining low EPC (0.2 ± 0.02) nm/cycle and low surface roughness of 0.3 nm. [19]

Finally, AlGaN/GaN HEMTs were fabricated using optimized ALE modes, which were successfully applied for gate [17] and ohmic contact recesses. A linear relationship between $V_{th}$ and etch depth can be demonstrated (Fig. 1b). For ohmic contact recess etching an optimum for certain recess depth could be achieved with significantly reduced contact resistance (< 0.2 Ωmm) for gold-based Ti/Al/Ni/Au stacks (Fig. 2) and allowed lower annealing temperatures, reducing thermal stress and improving CMOS compatibility.

The combination of robust chamber cleaning and conditioning, rapid ALE recipes demonstrate a cost-efficient and sustainable tool to optimize the device performance of conventional lateral HEMT devices.

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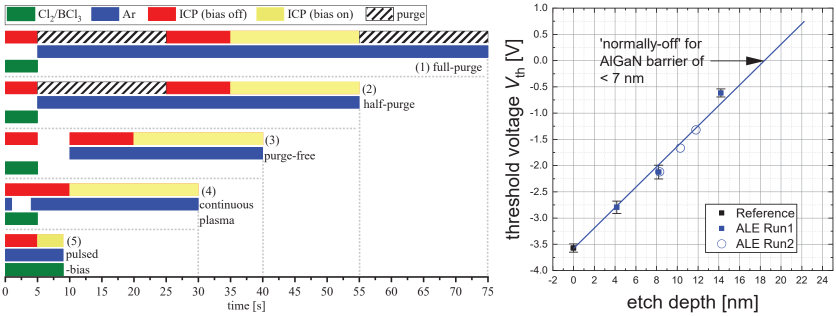

Fig 1. (a) Cycle sequence over time for the five different ALE modes. (b) Threshold voltage $V_{th}$ extracted from step in gate capacitance. $V_{th}$ increases linearly with etch depth.

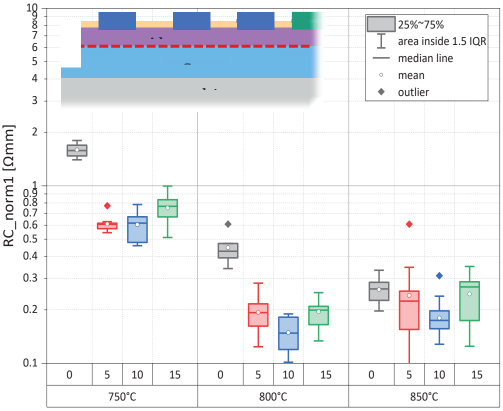

Fig 2. Results of electrical characterization of recessed ohmic contacts. Reducing the contact resistance for 750 °C, 800 °C and 850 °C annealing temperature with visible trend and optimum is achieved at 10 nm recess etch.

# Investigation of Au-Si Eutectic Bonding for MEMS Wafer-Level Packaging Application

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## Abstract

Eutectic Au–Si bonding enables strong, hermetic, and electrically conductive interfaces for microsystem packaging and heterogeneous integration. It relies on a transient liquid phase above 363 °C, promoting effective wetting and adhesion between gold and silicon. Au–Si bonds combine low process temperature with high electrical and thermal conductivity, chemical stability, and semiconductor compatibility. However, liquid-phase confinement is challenging, risking alloy squeeze-out. We investigate eutectic bonding at 390 °C and solid-state bonding at 350 °C on crystalline (c-Si) and amorphous silicon (a-Si), evaluating bond strength via compression shear testing.

## Materials and Methods

This study examines the bond strength of 1000 nm Au bonded to 200 nm amorphous and crystalline silicon (a-Si and c-Si) as a function of pre-bond treatment, bonding pressure, bonding time, and post-bond annealing. Experiments were conducted on 10 x 100 mm coupons using an EVG 540 bonder with a stainless-steel adapter wafer and graphite-film. Post-bond annealing (PBA) at 300 °C for 30 min was evaluated. The bonded coupons were then diced, and the resulting chips were subjected to compression shear testing using a TIRA shear tool to quantify bond strength.

## Results and Discussion

*Influence of pretreatment on a-Si & c-Si:*

For eutectic Au/Si bonds formed at 390 °C (fig. 1), BHF pretreatment leads to similar shear strengths for both a-Si and c-Si with larger spread of the data for Au/c-Si bond. In contrast, without BHF pretreatment, Au/a-Si exhibits significantly higher bond strength than Au/c-Si, indicating that amorphous silicon is less sensitive to native oxide formation and interfacial contamination.

*Process optimization for Au/c-Si bonding:*

Building on the pretreatment effects, Au/c-Si stack is further evaluated in fig. 2a. An influence on bond strength between solid-state bonding at 350 °C and eutectic bonding at 390 °C using BHF pretreatment, with and without post-bond annealing (PBA) is conducted. Eutectic bonding at 390 °C consistently results in higher shear strength than solid-state bonding at 350 °C. In both cases, PBA at 300 °C for 30 min further increases the bond strength. Fig. 2b illustrates that for eutectic Au/c-Si bonding at 390 °C without pretreatment, the highest bond strength is achieved at a moderate pressure of 10 MPa. The anisotropic reaction of c-Si with Au at 20 MPa is assumed to cause excess squeeze-out that degrade uniformity [2]. Post-bond annealing increases shear strength at both 10 MPa and 20 MPa. Results indicate that moderate pressure combined with PBA is optimal for non-pretreated c-Si.

*Influence of bond pressure on Au/a-Si eutectic bonds at 390 °C:*

The Au/a-Si eutectic bonds formed at 390 °C with BHF pretreatment show a strong dependence on bond pressure (fig. 3): mean shear strength increases from ~30 MPa at 5–10 MPa to ~73 MPa at 20 MPa, suggesting enhanced Au–Si interdiffusion and improved interfacial cohesion at higher pressures.

## Conclusion

Eutectic Au–Si bonding at 390 °C consistently achieves higher shear strength than solid-state bonding at 350 °C, with post-bond annealing further enhancing bond strength. Across the tested conditions, amorphous silicon either matches or surpasses crystalline silicon in shear strength and shows reduced sensitivity to pretreatment, highlighting its superior process tolerance.

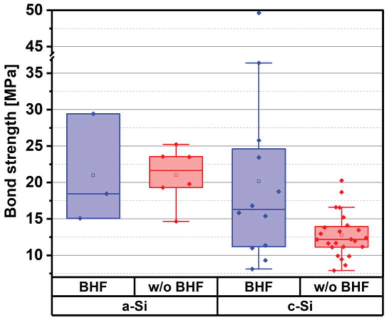

**Fig. 1:** Influence of BHF pretreatment on the shear strength of Au–Si eutectic bonds on a-Si and c-Si (a-Si: 200 nm; Au: 1000 nm; Bond temperature/ pressure/ time: 390 °C/ 5 MPa/ 15 min)

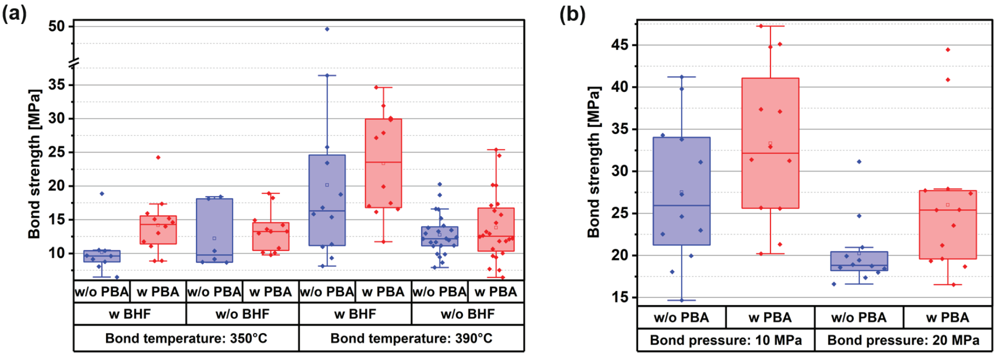

**Fig. 2:** Process optimization for Au/c-Si bonding: **(a)** Effect of solid-state (350 °C) and eutectic (390 °C) bonding with BHF pretreatment and post-bond anneal (PBA) (Au: 1000 nm; Bond pressure/ time: 5 MPa/ 15 min) and **(b)** Influence of bond pressure and PBA on eutectic bonds at 390 °C without c-Si pretreatment (Au: 500 nm; Bond time: 15 min)

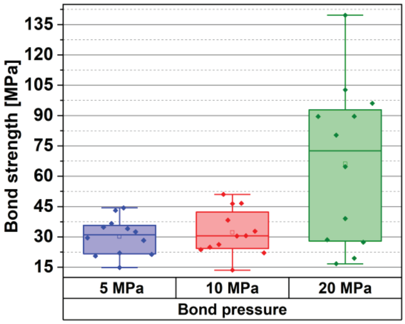

**Fig. 3:** Influence of bond pressure on Au/a-Si eutectic bonds at 390 °C (Au:a-Si = 500:200 nm; Bond time: 15 min, with a-Si pretreatment), showing a significant increase in shear strength.

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# Data-driven resolution of processability issues in technology scale-up

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During a technology industrialization, a processability issue has been critically analyzed and possible factors have been rationalized. By focusing on detection strategy, a methodology to address the solution was defined and improvements evaluated. Indeed, not relevant issues during development phase can have a significant impact upon new technologies industrialization as production volumes increase. The low frequency occurrence makes it difficult to correlate with a specific cause and a trial-and-error approach is inefficient. However, by performing attentive data analysis, the effects of corrective actions can be evaluated, reducing the number of required trials.

During the industrialization of a technology, a processability issue was observed in barrier and seed PVD deposition process due to sequencer failures. The process is done on multichambered cluster. When the handler moves wafers from and to different chambers, it determines whether the wafer is centered in the expected position or adjustments have to be made. The required adjustments are represented by the LCF (Local Center Finder) value in μm: when it exceeds 2500 μm, the tool shows a warning, when it exceeds 5000 μm, the tool issues a fault and wafer movement stops.

A first impact assessment was performed to address the magnitude and frequency of the faults. The worst performing tool exhibited ca.1% failure rate, resulting in 12 failures/day estimation in a scenario where only this technology is processed. To better understand the problem, a dedicated FDC (Fault Detection Control) was developed to extract and analyze LCF data for all wafers from every chamber. This data analysis enabled comparison of the failing parameter across different technologies, improving the process of root cause identification and providing a method to evaluate problem resolution effectiveness of corrective actions.

Comparing the failing technology to a reference technology, LCF data resulted more dispersed for the failing one as shown in Fig. 1. Comparing different chambers used in the barrier/seed process, only the ones using electrostatic chucking during the process were found to determine the increase in the LCF spread and cause the faults. Based on industrial knowledge of processability problems in chambers with chucks, different trials were proposed and evaluated by changing parameters related to de-chuck values. Chucking efficiency depends on various factors, such as differences in the wafer's back composition, which could also explain the different behaviors by technology. Dependence on specific substrates makes reproducing the problem difficult, as test wafers are not representative and only production lots can be used.

Trials were conducted to evaluate an improvement in the LCF data. As shown in Figure2, trials performed on chamber type "A" never lead to processability issue indeed LCF data distribution almost halved by reducing it below the warning value while for the chamber type "B" new trials have to be performed.

An effective approach to face with processability issues has been developed, including the definition of an effective detection strategy, of proper test vehicle and trial protocol, as well as a methodology for attentive data analysis and for setup of process optimization trials. Accordingly, a best practice has been acquired and it will be applied for all new technologies introduction.

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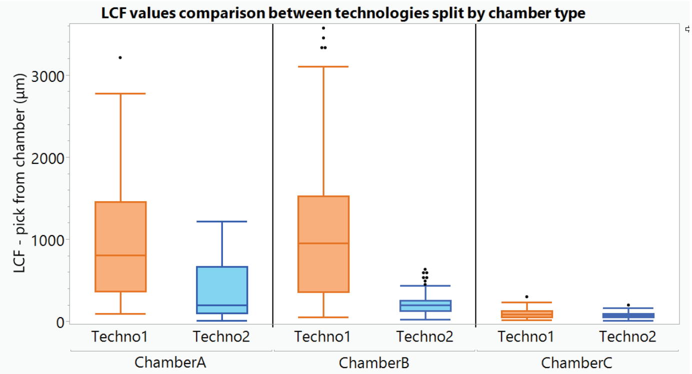

*Fig. 1: LCF values extracted for two different technologies and plotted split by different chambers used in the barrier/seed process. Techno1= failing technology, Techno2= reference technology*

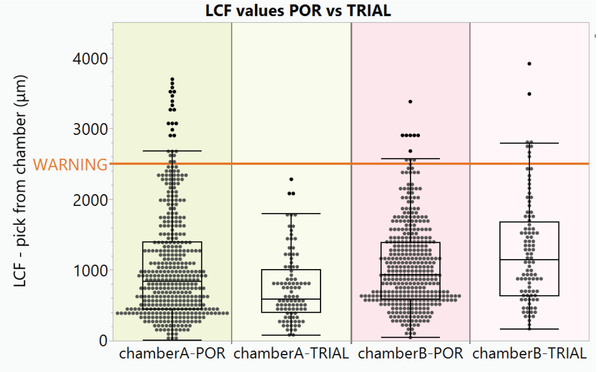

*Fig. 2: LCF values collected from 430 samples by using POR recipes and 85 samples from TRIAL recipes divided by chamber type "A" and "B"*

# Simulation of Metal-Assisted Halogen-Free Etching of Silicon Using Ruthenium Catalyst

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## Introduction

Silicon (Si) is the foundational material of modern micro- and nanotechnology, requiring precise nanoscale etching for device fabrication [1]. Si etching methods include wet chemical etching, metal-assisted chemical etching, and plasma-based techniques such as reactive ion etching (RIE), which enable selective removal of unmasked silicon using metal masks (e.g., Al, Au, Cu) with control over anisotropy, selectivity, and etch rate. Mask-enhanced etching beyond conventional RIE has been reported, where metals such as Al, Cu, Ag, and Au locally enhance Si etching due to an increased local concentration of fluorine radicals near the metal surface, accelerating the formation of volatile silicon tetrafluoride ($SiF_4$) [2], forming the basis of metal-assisted plasma etching. Plasma etching proceeds through reactive species, including ions and radicals, that remove material from the surface.

Conventional Si etching using fluorinated gases such as $SF_6$ and $CF_4$ achieves high etch rates but generates per- and polyfluoroalkyl substances (PFAS) and greenhouse gases. Hydrogen-based plasma etching produces volatile silane ($SiH_4$) instead of $SiF_4$ but exhibits low silicon etch rates due to the high activation energy for hydrogen dissociation. In this work, we hypothesize that a catalytic metal such as Ru enhances molecular hydrogen dissociation, generating reactive atomic hydrogen and increasing the Si etch rate.

## Result and discussion

$H_2$ dissociation on a $Ru_{14}$ cluster was investigated by initially placing the $H_2$ molecule 4.8 Å from the cluster. The calculated reaction energy profile shows a barrierless dissociation process with a final-state energy of -1.8 eV (−0.9 eV per H atom), consistent with reported dissociative adsorption energies of −0.91 eV for $H_2$ on Ru surfaces [4]. Previous studies of $H_2$ dissociation on the Si (100) surface have identified intra-dimer and inter-dimer pathways, with the lowest activation barrier associated with the inter-dimer pathway [5].

$H_2$ dissociation on Si (100) surface and surface with $Ru_{14}$ were also investigated. On the clean Si (100) surface, dissociation proceeds via an activation barrier of $E_a$ = 0.33 eV, consistent with reported DFT values in the range of 0.3–0.7 eV [5], and follows the intra-dimer pathway. In contrast, on the Si–Ru surface, a barrierless dissociation pathway is observed via the inter-dimer configuration. The reaction energies for $H_2$ dissociation on clean Si and Si–Ru surfaces are −1.86 eV and −1.9 eV, respectively, indicating that Ru promotes efficient hydrogen dissociation and provides a localized source of atomic hydrogen at the metal–silicon interface.

The etching of silicon via the formation of volatile silane ($SiH_4$) from a clean Si surface was examined by considering two distinct reaction pathways. In the first pathway, a high-energy hydrogen atom originating from the plasma directly attacks a surface-bound $SiH_3$ species. As shown by the dotted red line in Fig. 2(b), this process leads to silicon etching through a barrierless reaction pathway. In the second pathway, an adsorbed hydrogen atom located on a neighbouring surface Si atom reacts with the adjacent $SiH_3$ species to form $SiH_4$. As indicated by the blue line in Fig. 2(b), this reaction proceeds via an activated process and requires overcoming an energy barrier of $E_a$ = 2.3 eV.

In contrast, when a Ru cluster is present on the Si surface, atomic hydrogen binds strongly at the Si-Ru interface, while the $SiH_3$ species becomes unstable (see Fig. 3), limiting spontaneous formation and desorption of volatile etch products. These results indicate that Ru primarily functions as an efficient hydrogen activation site rather than directly facilitating silicon removal, clarifying its role in halogen-free plasma etching.

## Methodology

An Si (100) surface was selected for modelling. The Si slab was generated using the Atomic Simulation Environment (ASE), visualized with VESTA (Fig. 1a), and consisted of 160 atoms, including surface reconstruction on the reactive side and hydrogen passivation of dangling bonds on the backside. A $Ru_{14}$

cluster with a double-layer hexagonal (hcp-like) structure was modelled using Avogadro (Fig. 1b) [3]. All geometries were fully relaxed to obtain minimum-energy configurations.

All energies and geometries were calculated using density functional theory (DFT) with the Quantum ESPRESSO package. Ultrasoft pseudopotentials from the Quantum ESPRESSO library were employed for all elements. Convergence tests yielded a plane-wave cutoff of 50 Ry for the wavefunction, 500 Ry for the charge density, and a 2 × 2 × 1 k-point mesh. Geometry relaxations used a self-consistency threshold of $1 \times 10^{-6}$ eV. Minimum-energy paths for $H_2$ dissociation and etching reactions were determined using the nudged elastic band (NEB) method.

Figure 1. (a) Optimized structure of the $Ru_{14}$ cluster. (b) Optimized structure of the $Ru_{14}$ on the Si (100) surface.

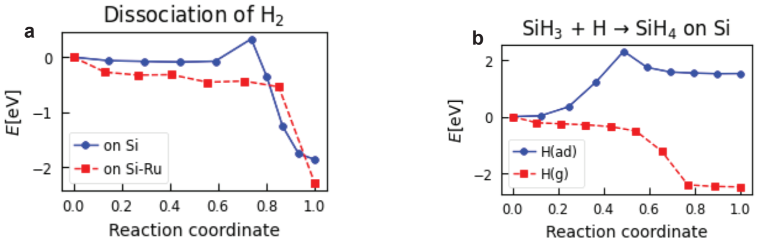

Figure 2. (a) Reaction pathway for $H_2$ dissociation on clean Si ($E_a$ = 0.33eV), and on the Si–Ru surface (barrierless). (b) Reaction pathway for the etching of Si on the Si surface with hydrogen adsorbed on a neighboring Si atom ($E_a$ = 2.3eV), and with a hydrogen atom originating from the gas phase (barrierless).

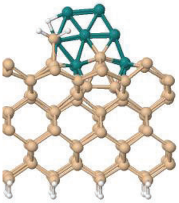

Figure 1. Optimized structure of $SiH_3$ on Si surface containing $Ru_{14}$ cluster

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# Advanced node process characterization: novel chemical mechanical polishing with environmentally friendly abrasive free setup

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For copper metallization chemical mechanical polishing (CMP) is necessary to enable damascene processing. To planarize and selectively remove copper in a bulk polish step established solutions are available but rely on relatively cost intense as well as hazardous and environmental unfavourable CMP slurry. A potential alternative are functionalized CMP pads enabling a significant copper material removal without the need of classical copper bulk slurry. As the pads are chemically functionalized there is no abrasive involved in the process at all. In this work we present the characterization of this new consumable/process alternative for advanced node damascene structures.

For qualification of the novel process alternative an industry standard consumable set for copper damascene processing was used as benchmark. Both the benchmark process as well as the novel abrasive free process were used to polish blanket and patterned wafers on a 300 mm AMAT Reflexion CMP tool. Patterned wafers were designed to qualify a wide design range down to 45 nm CD typical for 28 nm technology.

Bulk polish performance was qualified for copper as well as typical BEoL stack materials (Tantalum barrier, SICOH and TEOS ILD). The tested abrasive free setup showed removal rates up to 850 nm/min for copper with very even removal over the wafer radius. Copper removal rate is slightly dependent on polish pressure allowing for profile control in manufacturing application (Fig. 1). Comparison to the POR polish showed similar copper removal rates with lesser within wafer non uniformity (without pressure control). Removal rates for barrier and ILD materials were negligible for both POR and alternative process, allowing a good stop on barrier performance.

Defect inspection on blanket wafers was challenging due to intense surface structures. SEM based defect review showed no pad residuals or critical scratches for wafers polished with the alternative process. The observed surface quality does not pose a critical challenge for the following barrier removal CMP step. Median of defect count with novel process is comparable or below POR value, with significant impact of slurry distribution (Fig. 2).

To compare the CMP performance on 28 nm node like structures patterned wafers with identical ILD, barrier and copper material were processed with both POR polish and alternative setup. Dishing in individual copper lines is known to be highly dependent on line width and density, thus values for a wide range of parameters were obtained. The novel process showed dishing values comparable to a standard polish (see Fig. 3). Small CD lines of 45 and 90 nm showed ~20 nm dishing, which is slightly more than the well-established POR (~5 and ~15 nm). The erosion of 45-450 nm CD line patterns was slightly less for the tested new consumable setup (see Fig 3). these CD lines, including those with wider widths, indicates values resembling to those of the POR, or in certain aspects, are less pronounced.

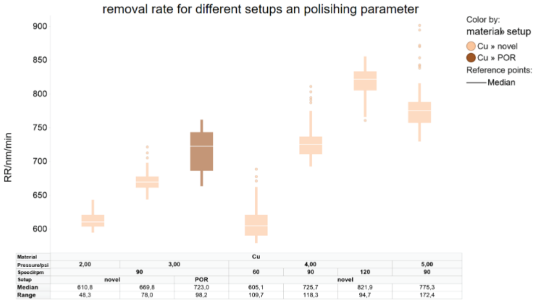

**Figure 1: Copper blanket wafer removal rate comparison between novel setup at different polish pressure and speed and POR. Box size indicates within wafer non uniformity.**

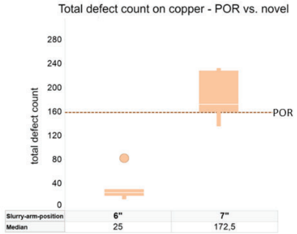

**Figure 2: Defect counts on blanket wafers for different slurry arm positions in comparison to POR.**

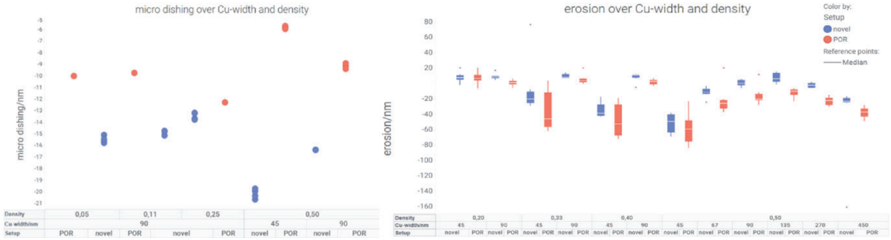

**Figure 3: Microdishing in individual 45 and 90 nm lines measured by AFM (left). Line erosion depending on density and CD measured by profiler scan (right).**

# Ultrafast Laser-Based Sample Preparation for Optimized FIB/SEM Workflows in High-Throughput Analysis

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With the increasing complexity of semiconductor devices, efficient and precise sample preparation has become essential for failure analysis, quality control, and advanced research and development. The microPREP® systems integrate ultrafast laser technology into the FIB/SEM workflow, enabling high-speed, athermal material ablation with micrometer-level accuracy. This approach significantly reduces preparation time from hours to minutes.

By employing ultrashort-pulse lasers, the system enables large-volume material removal with minimal thermal effects.[1] This capability is particularly beneficial for applications such as FIB trenching[2], atom probe tomography (APT) microtip fabrication[3], and cross-sectioning of advanced semiconductor packages[2]. Integration with xenon (Xe) plasma FIB-SEM systems establishes a hybrid workflow in which laser ablation performs bulk material removal, followed by high-precision FIB polishing for final refinement, thereby optimizing throughput.[1, 2, 3, 4]

This laser-based methodology is particularly impactful in semiconductor manufacturing, where speed, repeatability, and accuracy are critical. Computer-aided design (CAD)-based targeting further enhances precision by enabling rapid access to specific regions of interest. Case studies, such as flip-chip package analysis[2] and atom probe tomography, demonstrate significant improvements in productivity and process control.

This study demonstrates that integrating femtosecond laser systems into semiconductor workflows transforms sample preparation and offers a scalable solution to meet the requirements of next-generation device analysis.

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# Towards a calibrated TCAD model of an AlGaN/GaN HEMT device

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Due to physical limitations of silicon-based semiconductor devices, like poor electrical stability under high temperature and electric fields, the use of III-V materials like GaN has a major focus in research [1]. An important use case of this material is the AlGaN/GaN high-electron mobility transistor (HEMT). The two-dimensional electron gas (2DEG) that forms at the hetero junction has outstanding properties for high-frequency and high-power electronics [2]. To accurately predict and understand the electrical behaviour of such devices TCAD-simulations can be employed for device-design and optimization, as well as verification of fabrication processes. We aimed to reproduce the experimental transfer and output characteristics of AlGaN/GaN-HEMTs (Fig. 1) by TCAD numerical simulations to identify the key factors and their sensitivity that contribute towards those characteristics.

The work was based on an example for a AlGaN/GaN HEMT provided by Sentaurus from Synopsys [3]. Most of the example's physics, including e.g. high field saturation, thermionic emission and a simplified piezoelectric polarisation model, were deemed essential for the replication of the baseline behaviour. The dimensions and doping levels of the layers, as stated by the specifications of the device, were adjusted to our device. Additionally, the documented value for the work function for Nickel-Gold Schottky contacts of around 5.1 eV was set [4].

For the threshold voltage the main contribution is the density of the 2DEG which mainly depends on the thickness and mole fraction of the AlGaN-layer. Another important factor was the Fe-doping in the buffer layer which was introduced as acceptor states 0.7 eV below conduction band [5] with a concentration of $1.2 \cdot 10^{18}$ $cm^{-3}$, in order to compensate the intrinsic charge carriers within the GaN-buffer that shift the threshold voltage towards higher reverse bias.

To achieve the off-current of the experimental device, which was multiple magnitudes higher than what was reached by the simulation, trap-assisted tunnelling (TAT) was implemented. As literature suggests it can be a reason for the experimentally observed leakage current [6]. For this, acceptor states at 0.5 eV below the conduction band with a density of $5 \cdot 10^{12}$ $cm^{-2}$ were added at the GaN-cap/AlGaN-interface that facilitated a tunnelling path through the GaN-cap- and AlGaN-barrier.

The on-current is influenced by the contact resistance which was measured at 3.2 Ω·mm for the device and by the sheet resistance that was modified by setting a constant mobility within the channel region of 2200 $cm^{2} \cdot V^{-1} \cdot s^{-1}$. This was done to fit the simulated data to the linear slope of the output characteristic as shown in

Fig. 2 b). A discrepancy remains at higher drain voltages where the experimental data shows a more prominent degradation of the current. While a better fit can be achieved by reducing the high field saturation velocity of the electrons with the channel region from $1.8 \cdot 10^{7}$ $cm \cdot s^{-1}$ to $6.4 \cdot 10^{6}$ $cm \cdot s^{-1}$, we assume that self-heating [7] is mostly responsible for this effect and will be investigated in the future.

With these modifications a high level of agreement between the simulated and experimental characteristics can be achieved as shown in

Fig. 2. The determined 2DEG density of $4.8 \cdot 10^{12}$ $cm^{-2}$ and a sheet resistance of 619 Ω/sq are both within the range that was determined experimentally for our devices. Thus, the TCAD AlGaN/GaN HEMT calibration was successfully allowing to support optimization and device design at the institute.

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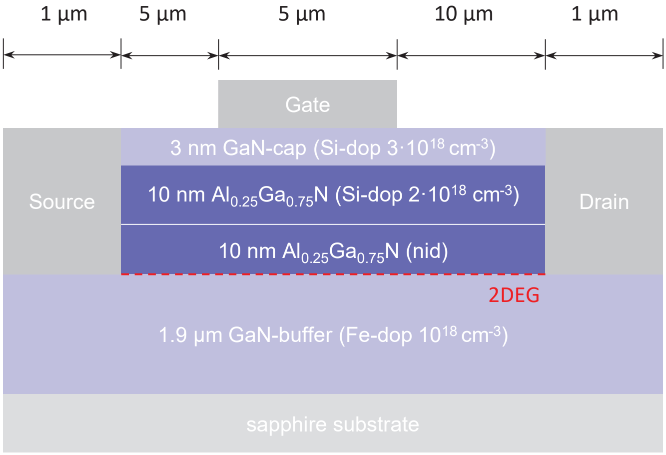

**Fig. 1 Basic structure of simulated AlGaN/GaN HEMT device**

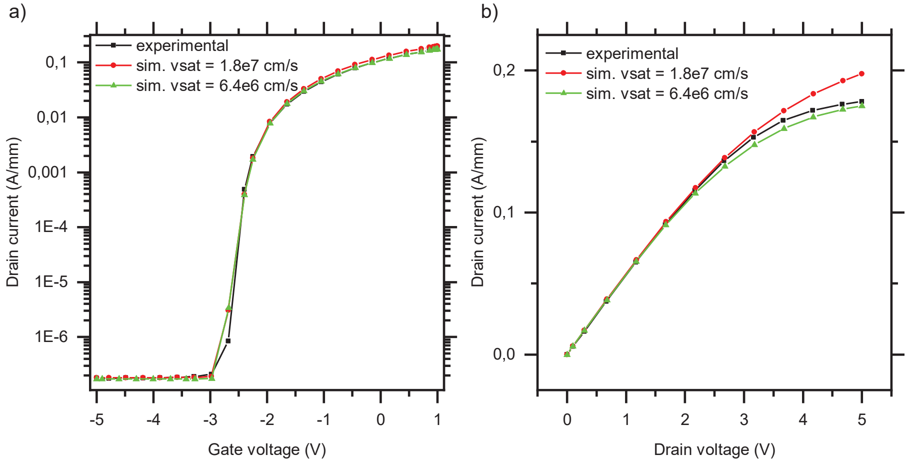

**Fig. 2 a) Transfer and b) output characteristic at 5 V drain-source voltage and 1 V gate voltage respectively; compares experimental data with simulated data with red – default high field saturation velocity and blue – reduced**

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